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35. M.2 CONN
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37. MISC:ITP/XTP CONN
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40. POWER TABLE
41. POWER SEQUENCE
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43. 3.3V
44. 2.5V / 1.2V / 0.6V
45. 1.8V
46. 1.7V / 1.5V / 1.3V
47. 1.05V
48. HISTORY

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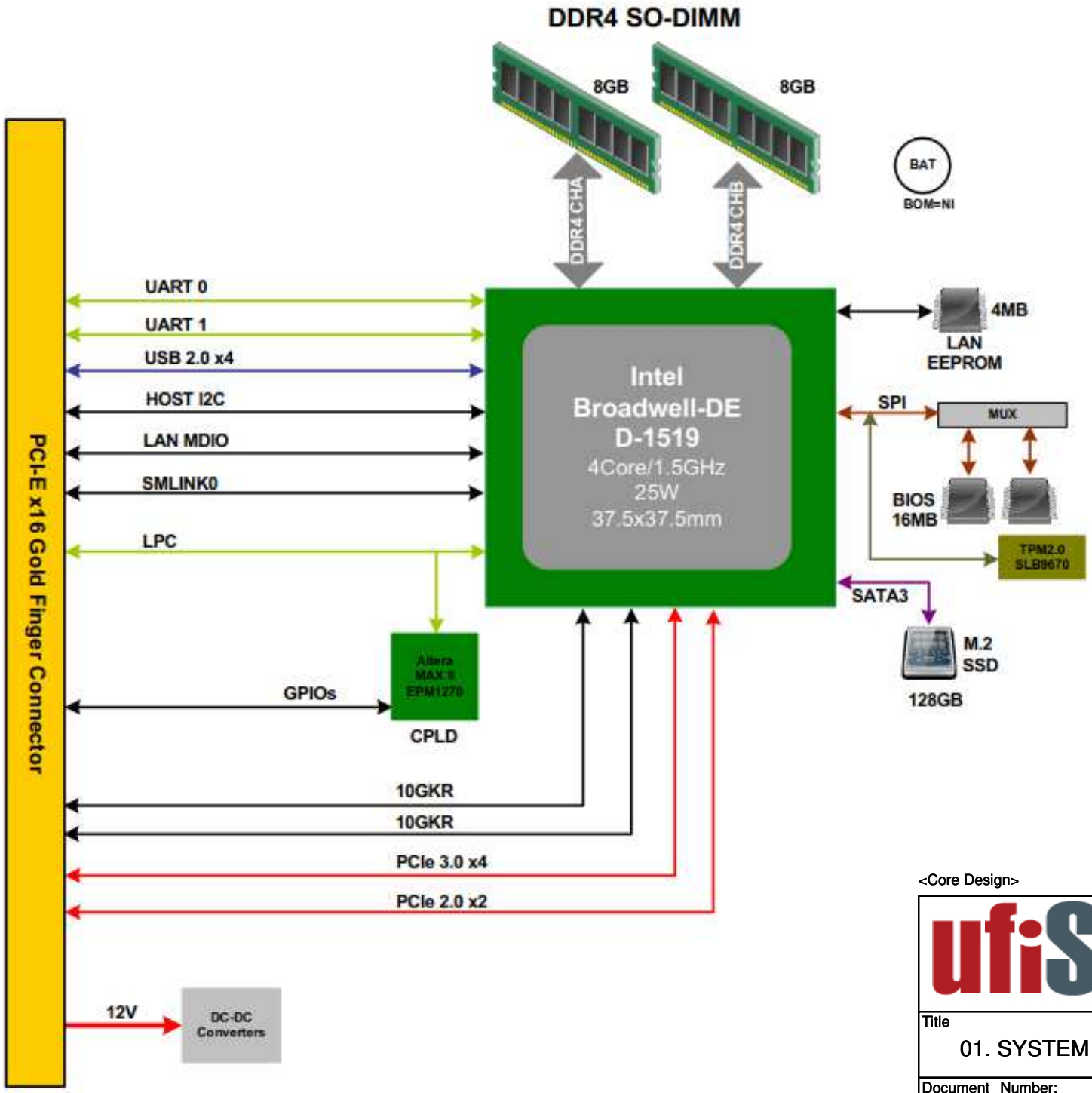
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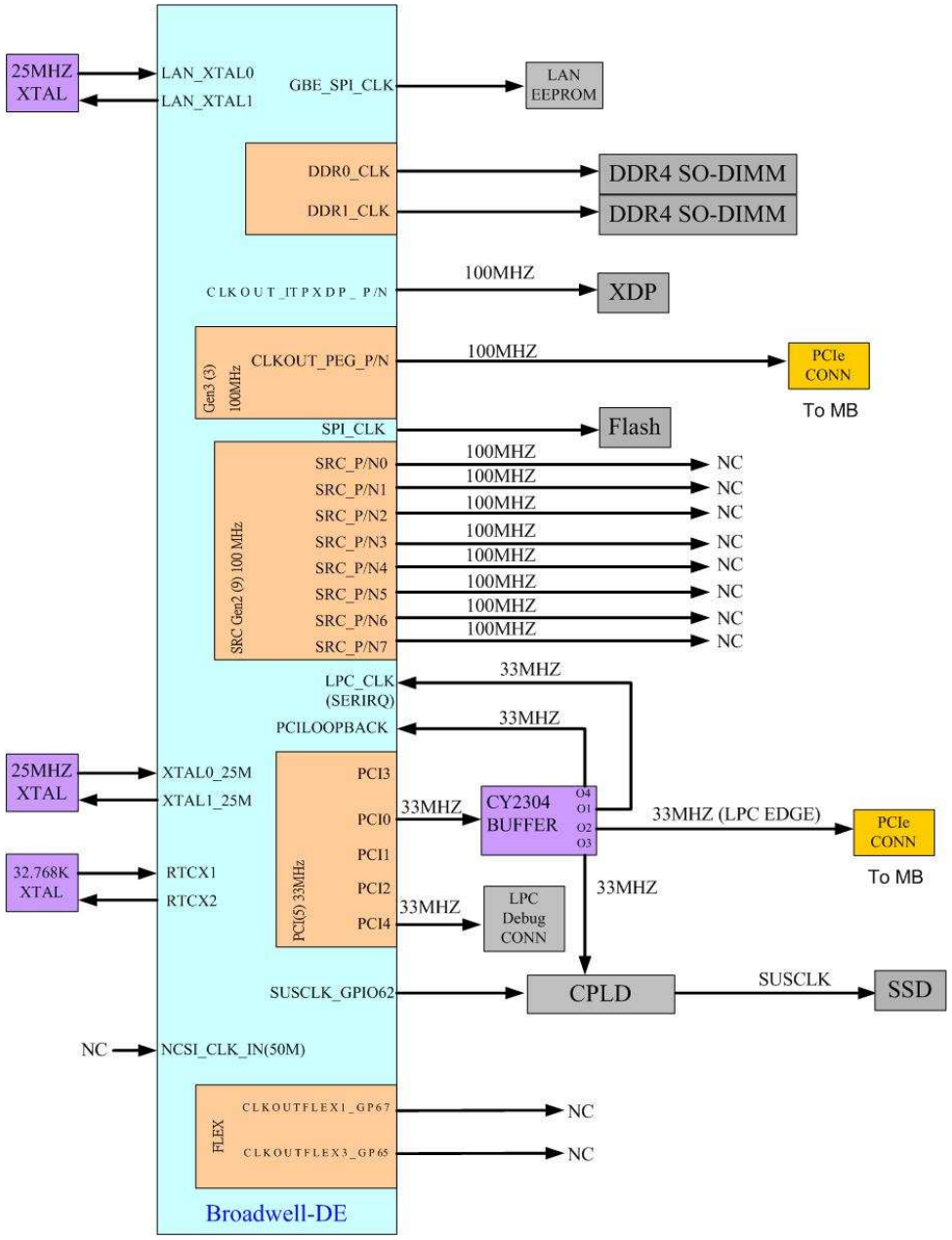
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Title

01. SYSTEM BLOCK DIAGRAM

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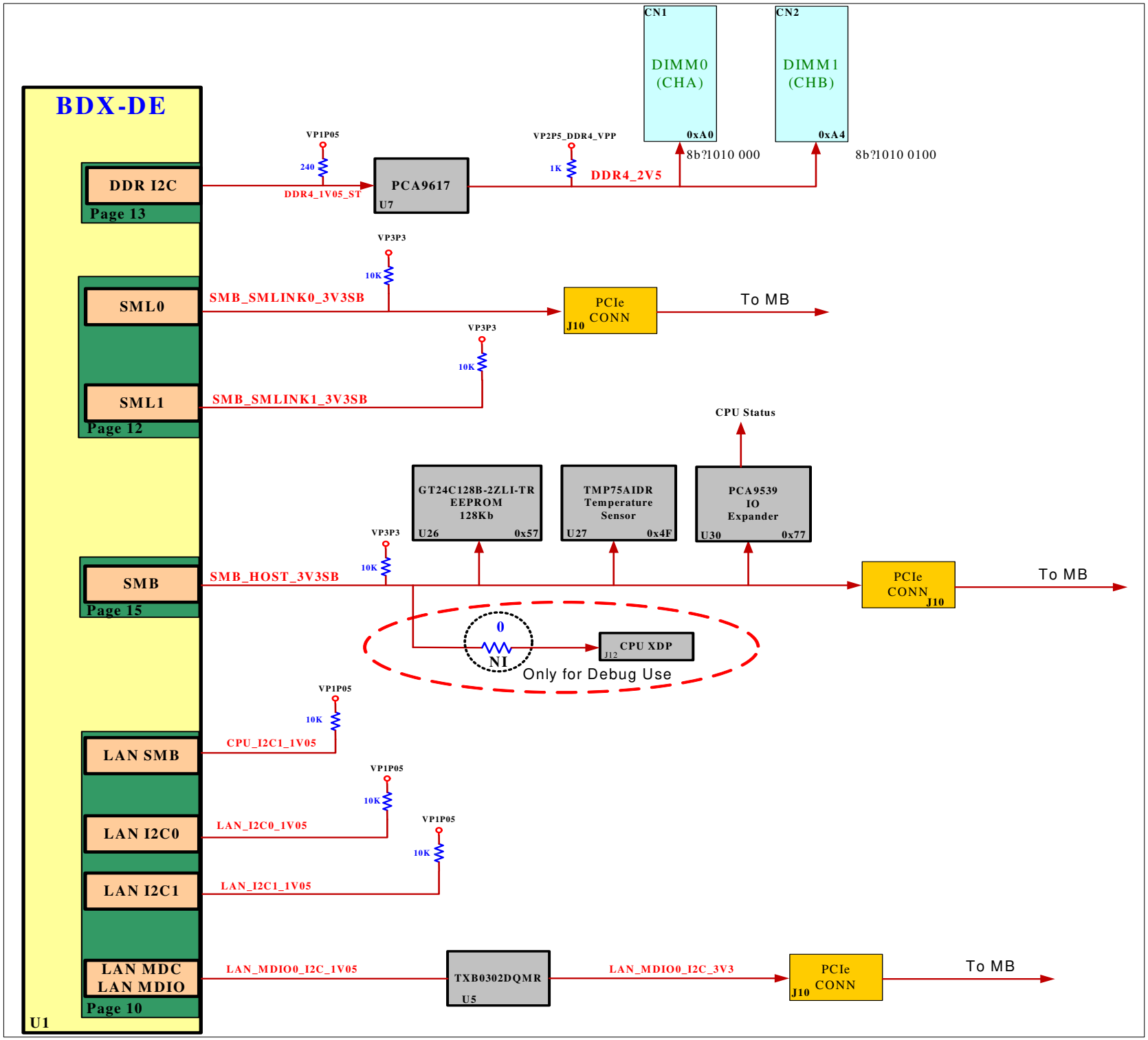


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Title: 03. CLOCK DIAGRAM

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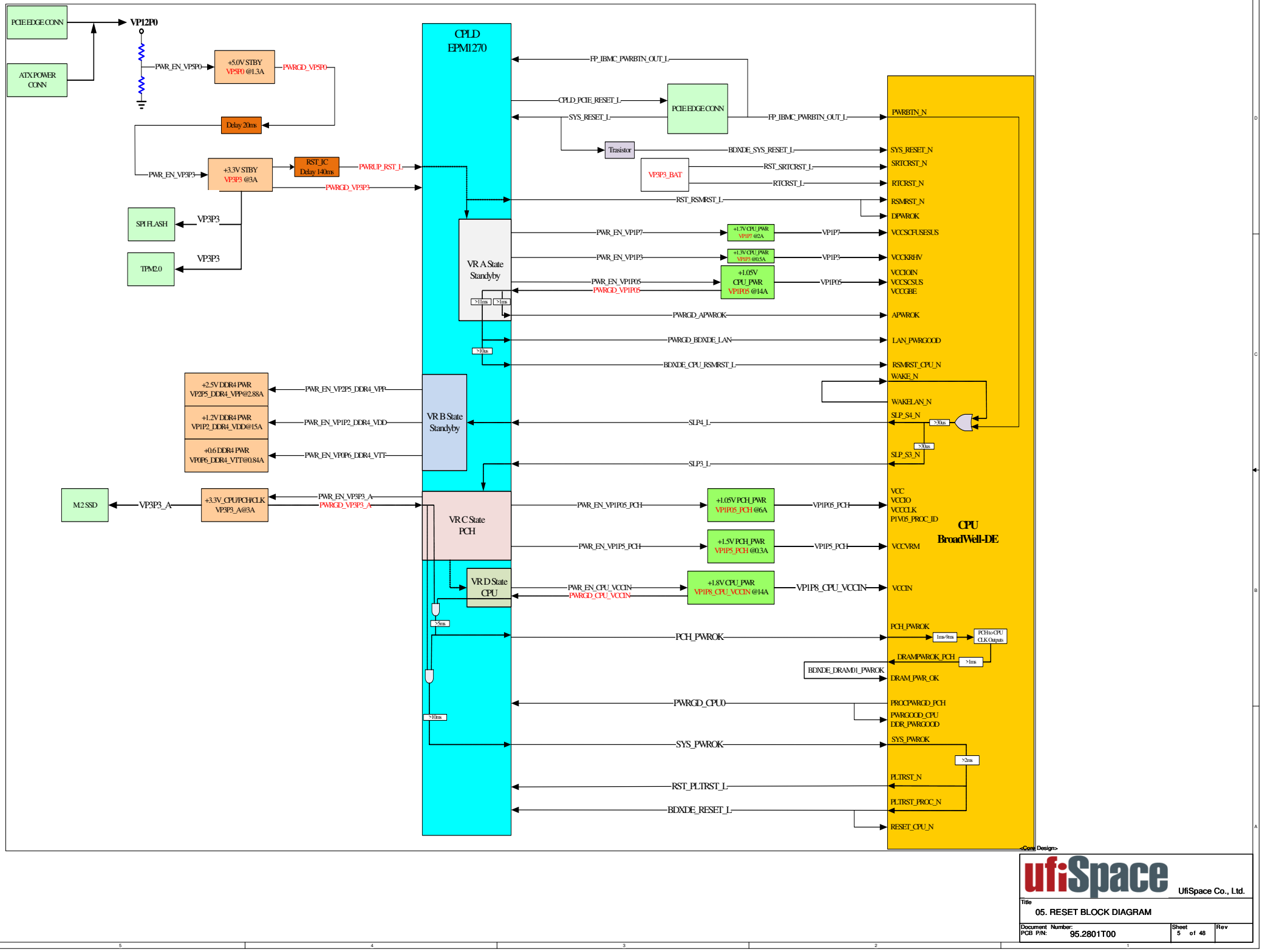
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Title: 04. SMB BLOCK DIAGRAM

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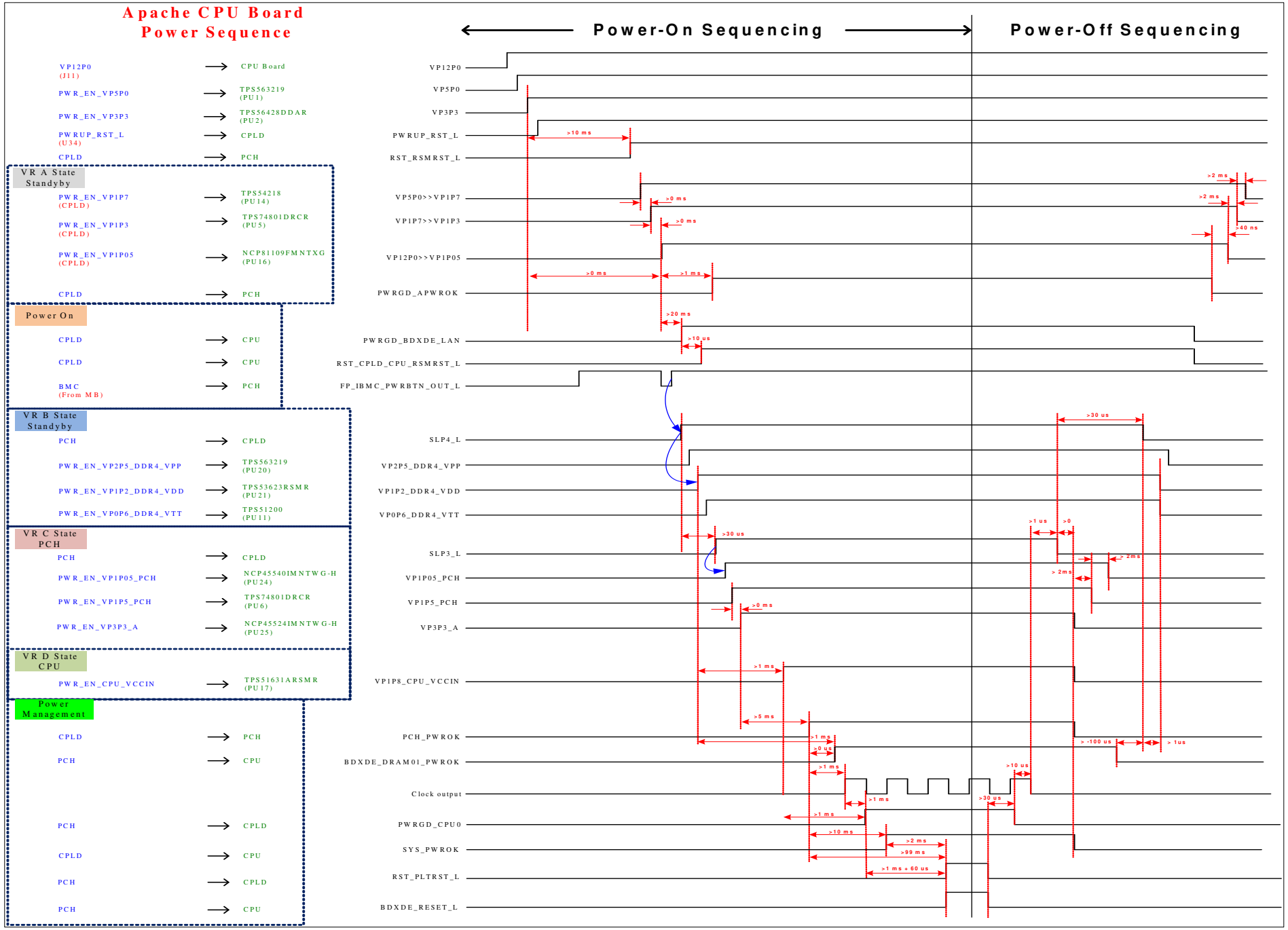
UfiSpace Co., Ltd.

Title

05. RESET BLOCK DIAGRAM

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Apache CPU Board Power Sequence



<Core Design>

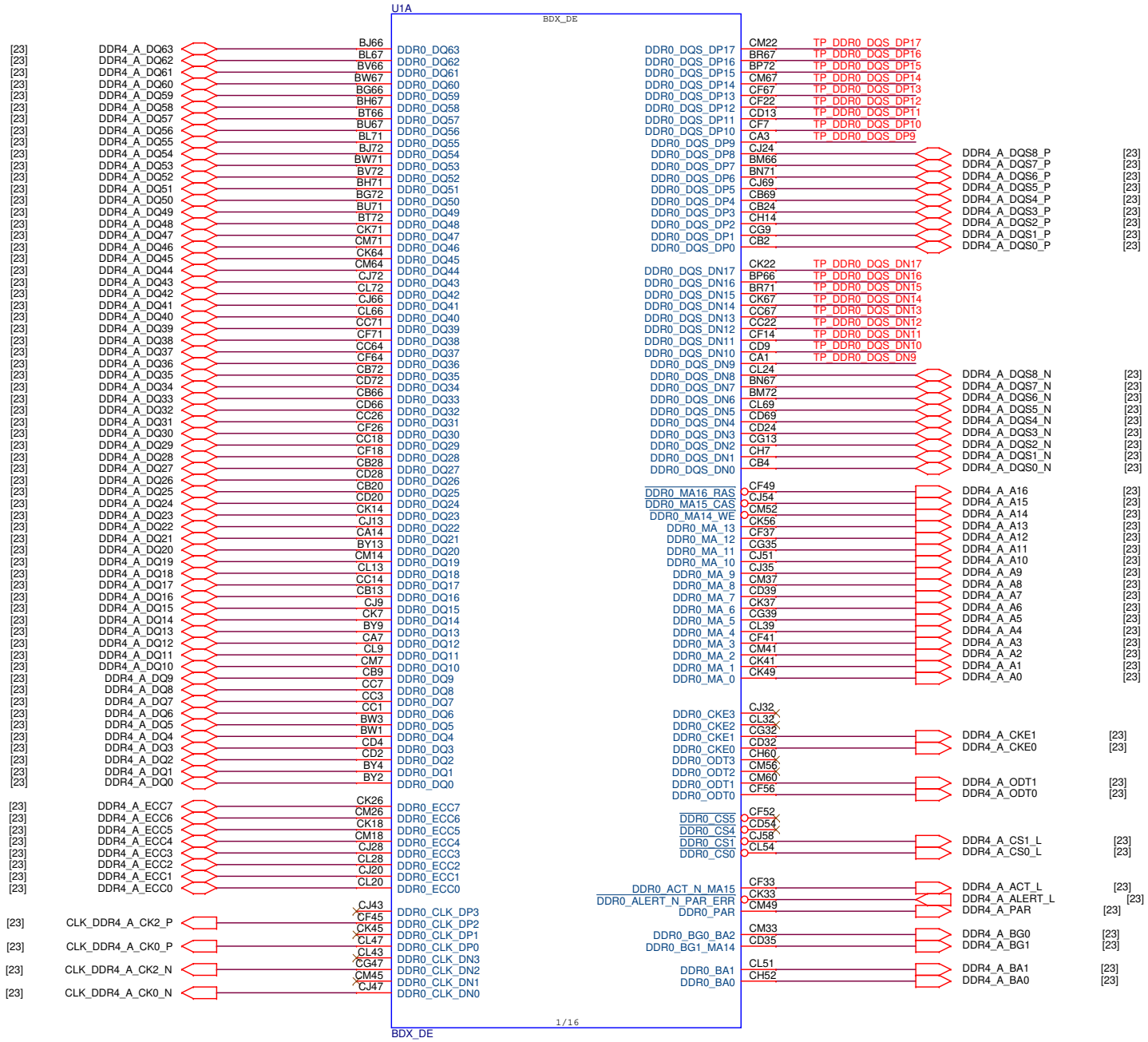
ufiSpace UfiSpace Co., Ltd.

Title: 06. POWER SEQUENCE

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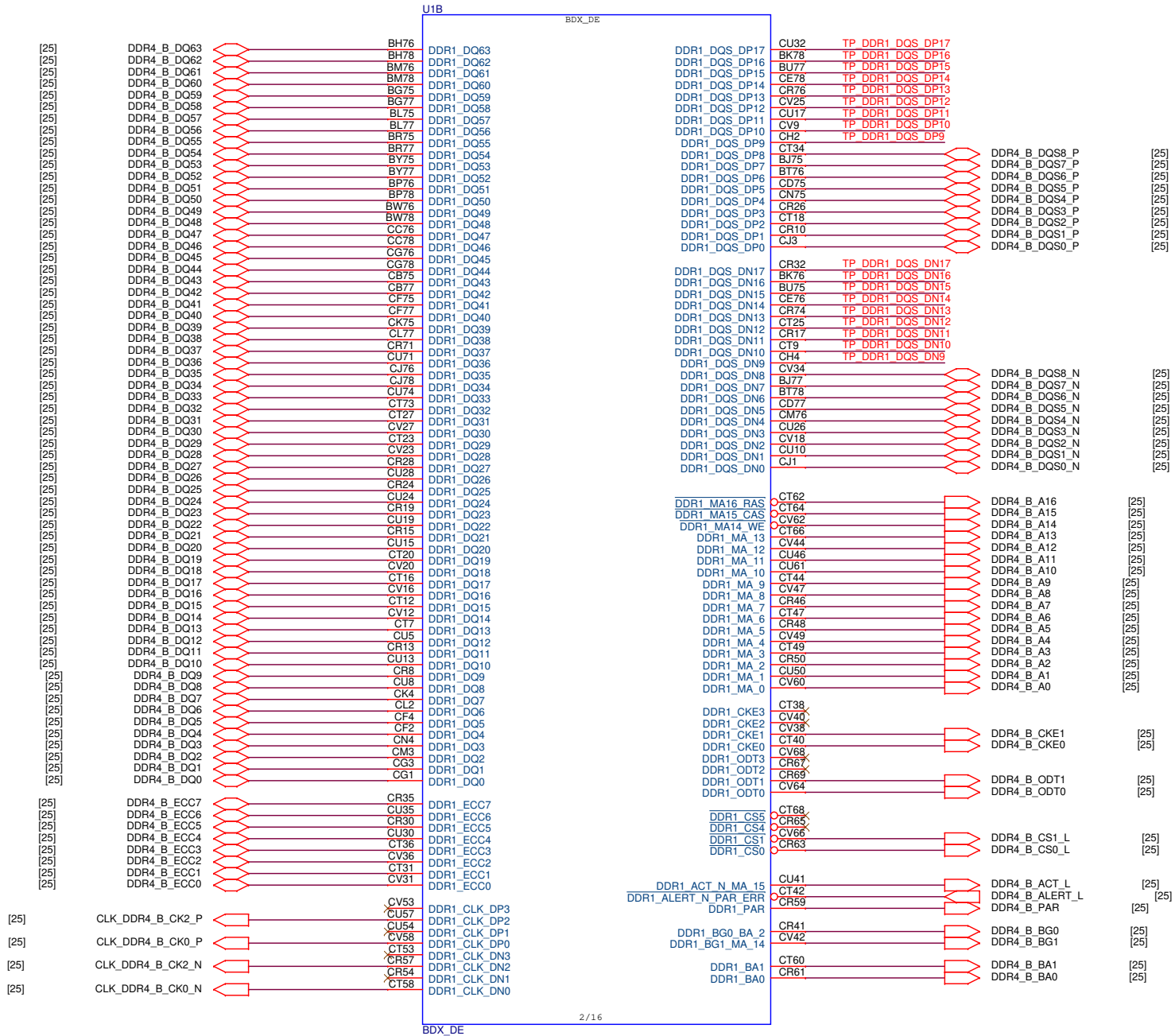
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Title

07. CPU DDR4 CHA

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<Core Design>

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Title

08. CPU DDR4 CHB

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<Core Design>

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Title: 09. CPU PCIE

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CAD:
TO PLACE CAPS CLOSE TO U1 LESS THAN 1"

2018/05/17: Remove LAN SMBus

10GE Port #	Device
0	10GE SWITCH
1	10GE SWITCH

2018/05/21
Add pull up resistors R468,R469,R472

<Core Design>

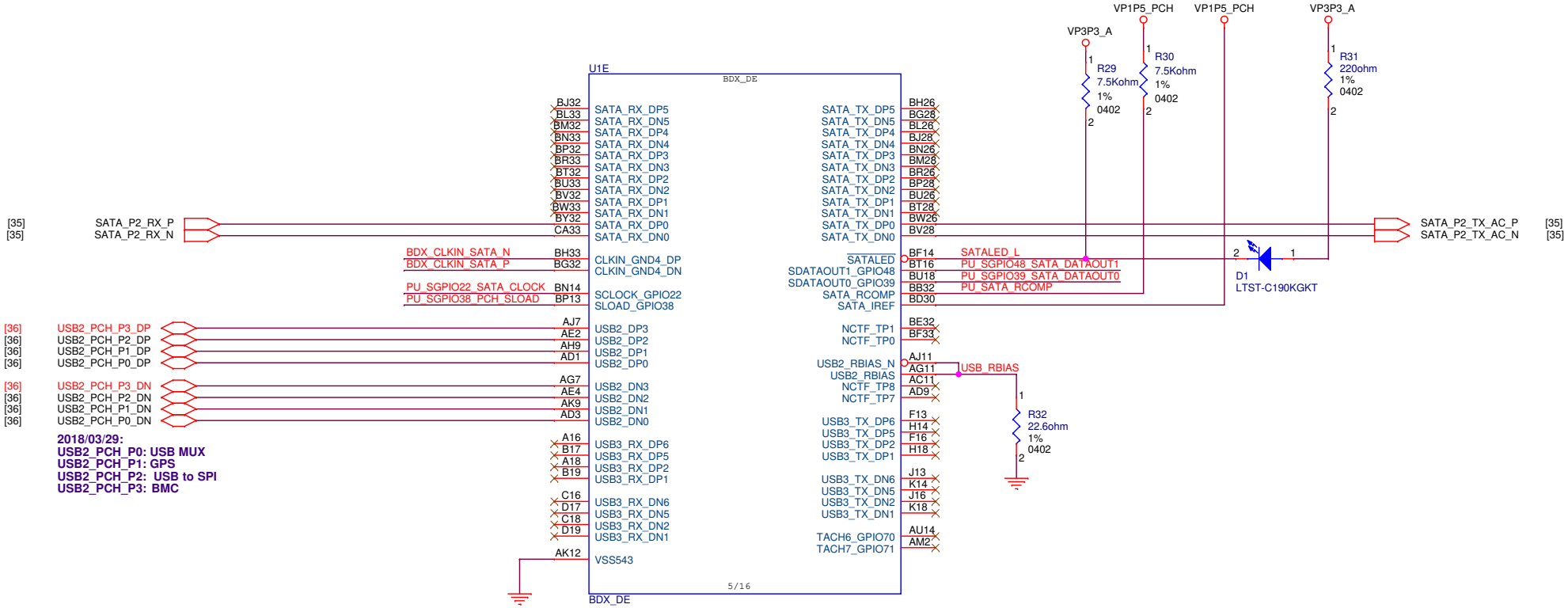
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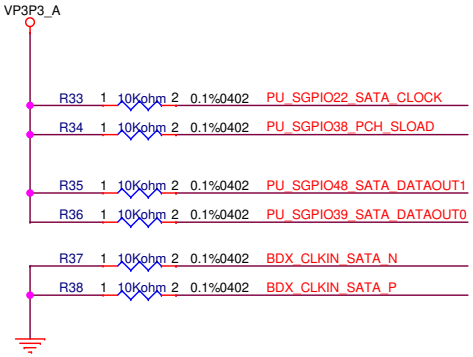
Title
10. CPU 10GBE LAN

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Device/Conn.	USB 2.0
GOLD FINGER CONN	0

CONN.	SATA
M.2 CONN	0
GOLD FINGER CONN	1

<Core Design>

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Title: 11. CPU SATA/USB

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Rev

FLASH DESCRIPTOR SECURITY OVERRIDE WHEN HIGH

2018/05/26 Need discuss with Eason

2018/05/17 Delete R39,R40

2018/05/26
Add R473

2018/09/26
Change to P3V3

LPC Debug Connector

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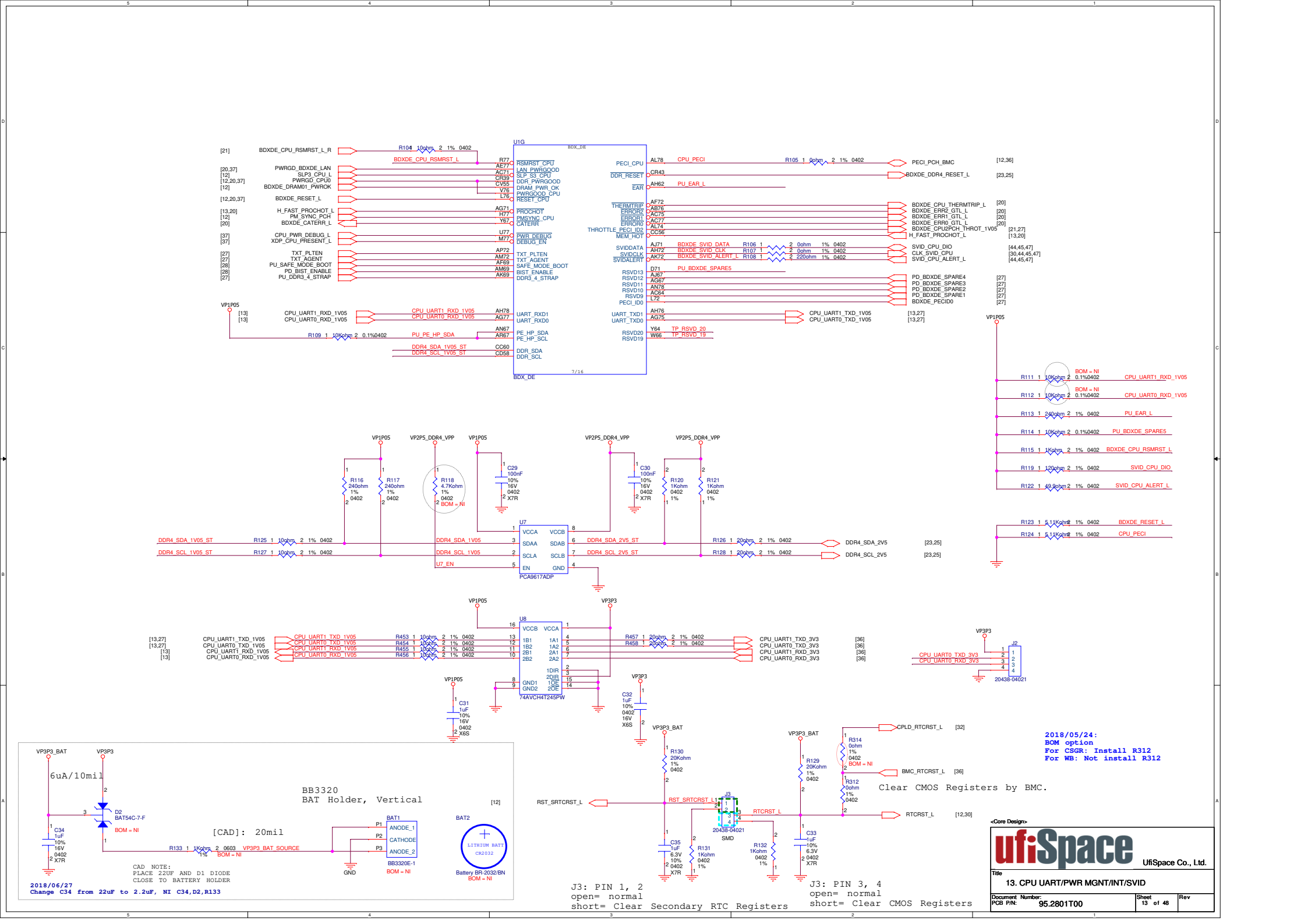
UfiSpace Co., Ltd.

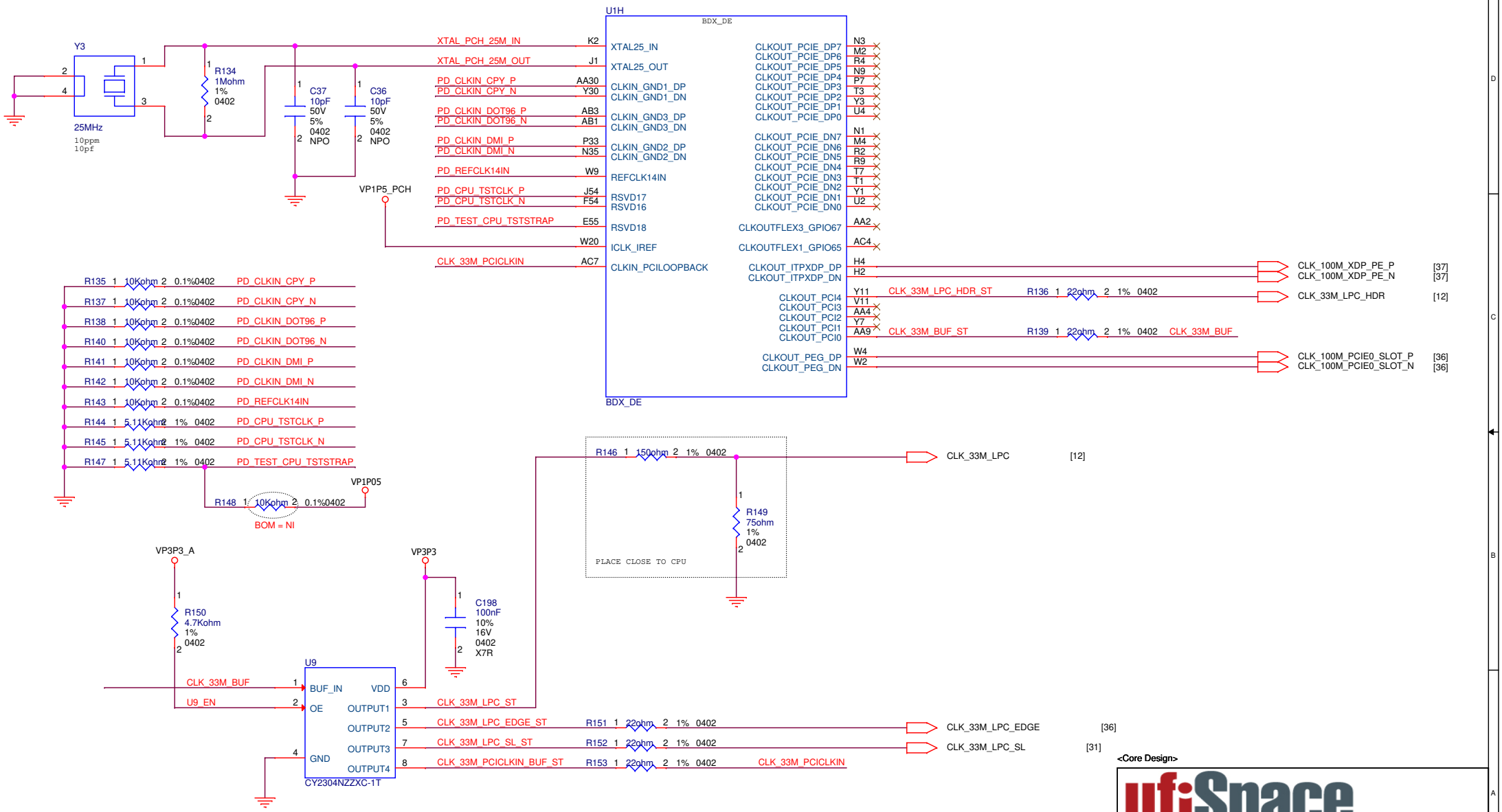
Title: 12. CPU LPC/SPI/GPIO/INT/PWR

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U1G
BDX_DE
BDXDE_CPU_RSMRST_L_R
R104 10ohm 2 1% 0402
BDXDE_CPU_RSMRST_L
PWRGD_BDXDE_LAN
SLP3_CPU_L
PWRGD_CPU0
BDXDE_DRAM01_PWROK
BDXDE_RESET_L
H_FAST_PROCHOT_L
PM_SYNC_PCH
BDXDE_CATERR_L
CPU_PWR_DEBUG_L
XDP_CPU_PRESENT_L
TXT_PLTEN
TXT_AGENT
PU_SAFE_MODE_BOOT
PD_BIST_ENABLE
PU_DDR3_4_STRAP
RSMRST_CPU
LAN_PWRGOOD
SLP_S3_CPU
DDR_PWRGOOD
DRAM_PWR_OK
PWRGOOD_CPU
RESET_CPU
PROCHOT
PMSYNC_CPU
CATERR
PWR_DEBUG
DEBUG_EN
TXT_PLTEN
TXT_AGENT
SAFE_MODE_BOOT
BIST_ENABLE
DDR3_4_STRAP
PECI_CPU
DDR_RESET
EAR
THERMTRIP
ERROR2
ERROR1
ERROR0
THROTTLE_PECI_ID2
MEM_HOT
SVIDDATA
SVIDCLK
SVIDALERT
RSVD13
RSVD12
RSVD11
RSVD10
RSVD9
PECI_ID0
UART_TXD1
UART_TXD0
RSVD20
RSVD19
CPU_PECI
PU_EAR_L
PU_BDXDE_SPARE5
TP_RSVD_20
TP_RSVD_19
PECI_PCH_BMC
BDXDE_DDR4_RESET_L
BDXDE_CPU_THERMTRIP_L
BDXDE_ERR2_GTL_L
BDXDE_ERR1_GTL_L
BDXDE_ERR0_GTL_L
BDXDE_CPU2PCH_THROT_1V05
H_FAST_PROCHOT_L
BDXDE_SVID_DATA
BDXDE_SVID_CLK
BDXDE_SVID_ALERT_L
SVID_CPU_DIO
CLK_SVID_CPU
SVID_CPU_ALERT_L
PD_BDXDE_SPARE4
PD_BDXDE_SPARE3
PD_BDXDE_SPARE2
PD_BDXDE_SPARE1
BDXDE_PECID0
CPU_UART1_RXD_1V05
CPU_UART0_RXD_1V05
CPU_UART1_TXD_1V05
CPU_UART0_TXD_1V05
PU_PE_HP_SDA
DDR4_SDA_1V05_ST
DDR4_SCL_1V05_ST
PE_HP_SDA
PE_HP_SCL
DDR_SDA
DDR_SCL
BDX_DE
VP1P05
R111 10Kohm 0.1%0402 BOM = NI
R112 10Kohm 0.1%0402 BOM = NI
R113 240ohm 1% 0402
R114 10Kohm 0.1%0402
R115 1Kohm 1% 0402
R119 120ohm 1% 0402
R122 49.9ohm 1% 0402
R123 5.11Kohm 1% 0402
R124 5.11Kohm 1% 0402
VP2P5_DDR4_VPP
R116 240ohm 1% 0402
R117 240ohm 1% 0402
R118 4.7Kohm 1% 0402 BOM = NI
C29 100nF 10% 16V 0402 X7R
C30 100nF 10% 16V 0402 X7R
R120 1Kohm 0402 1%
R121 1Kohm 0402 1%
U7
VCCA VCCB
SDAA SDAB
SCLA SCLB
EN GND
PCA9617ADP
R125 10ohm 2 1% 0402
R127 10ohm 2 1% 0402
R126 20ohm 2 1% 0402
R128 20ohm 2 1% 0402
DDR4_SDA_2V5
DDR4_SCL_2V5
VP3P3
U8
VCCB VCCA
1B1 1A1
1B2 1A2
2B1 2A1
2B2 2A2
1DIR
2DIR
GND1 1OE
GND2 2OE
74AVCH4T245PW
R453 10ohm 2 1% 0402
R454 10ohm 2 1% 0402
R455 10ohm 2 1% 0402
R456 10ohm 2 1% 0402
R457 20ohm 2 1% 0402
R458 20ohm 2 1% 0402
CPU_UART1_TXD_3V3
CPU_UART0_TXD_3V3
CPU_UART1_RXD_3V3
CPU_UART0_RXD_3V3
J2
20438-04021
C31 1uF 10% 16V 0402 X6S
C32 1uF 10% 0402 16V X6S
VP3P3_BAT
R130 20Kohm 1% 0402
R129 20Kohm 1% 0402
R314 0ohm 1% 0402 BOM = NI
R312 0ohm 1% 0402
CPLD_RTCRST_L
BMC_RTCRST_L
RTCRST_L
RST_SRTCRST_L
J3
20438-04021
SMD
C35 1uF 6.3V 10% 0402 X7R
R131 1Kohm 0402 1%
R132 1Kohm 0402 1%
C33 1uF 10% 6.3V 0402 X7R
6uA/10mil
D2 BAT54C-7-F
BOM = NI
C34 1uF 10% 16V 0402 X7R
R133 1Kohm 1% 0603 VP3P3_BAT_SOURCE
BOM = NI
[CAD]: 20mil
BB3320
BAT Holder, Vertical
BAT1
ANODE_1
CATHODE
ANODE_2
BB3320E-1
BOM = NI
BAT2
LITHIUM BATT
CR2032
Battery BR-2032/BN
BOM = NI
GND
CAD NOTE:
PLACE 22UF AND D1 DIODE
CLOSE TO BATTERY HOLDER
2018/06/27
Change C34 from 22uF to 2.2uF, NI C34,D2,R133
2018/05/24:
BOM option
For CSGR: Install R312
For WB: Not install R312
Clear CMOS Registers by BMC.
J3: PIN 1, 2
open= normal
short= Clear Secondary RTC Registers
J3: PIN 3, 4
open= normal
short= Clear CMOS Registers
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ufiSpace
UfiSpace Co., Ltd.
Title
13. CPU UART/PWR MGNT/INT/SVID
Document Number:
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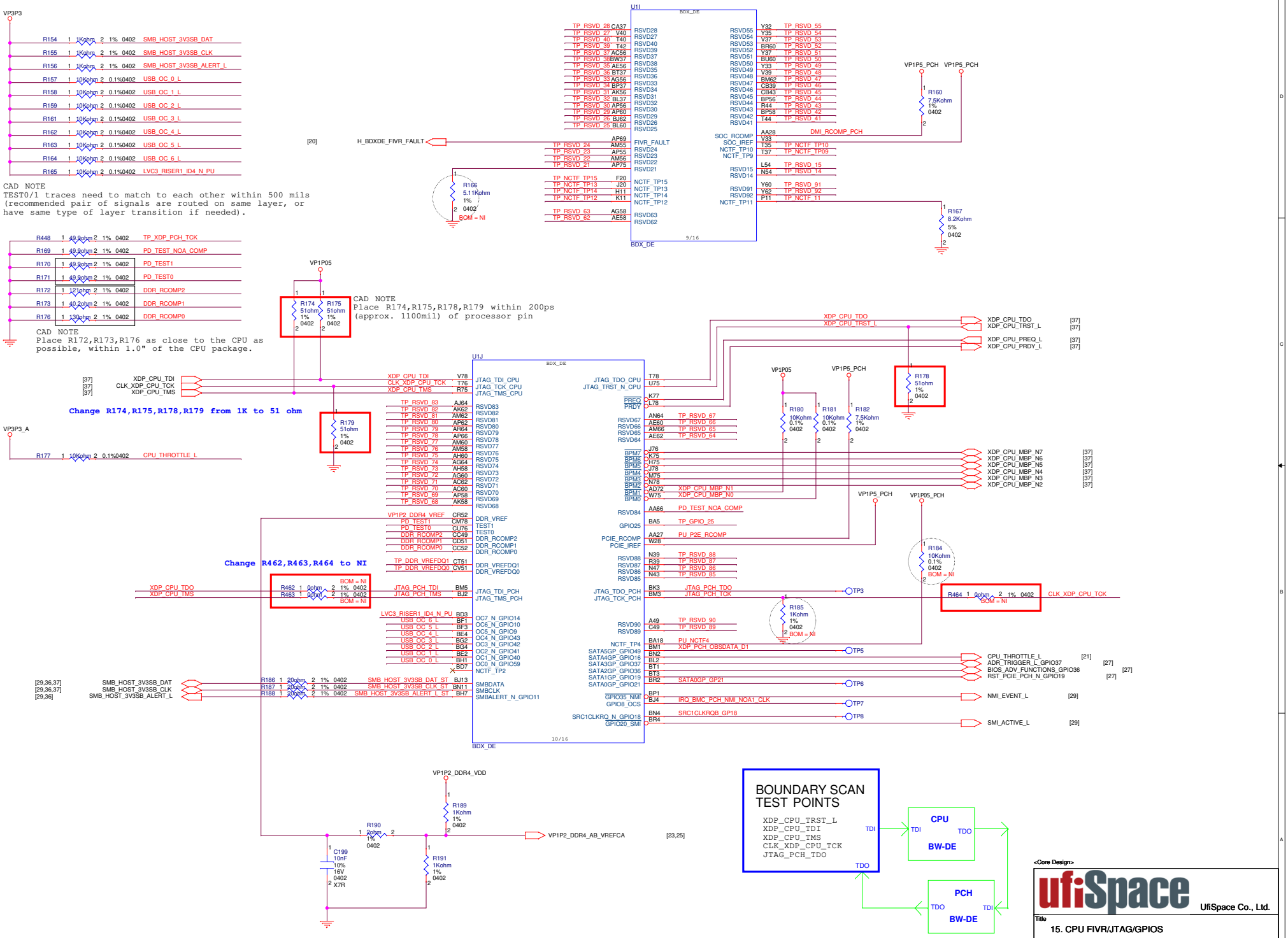
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Title

14. CPU CLOCK

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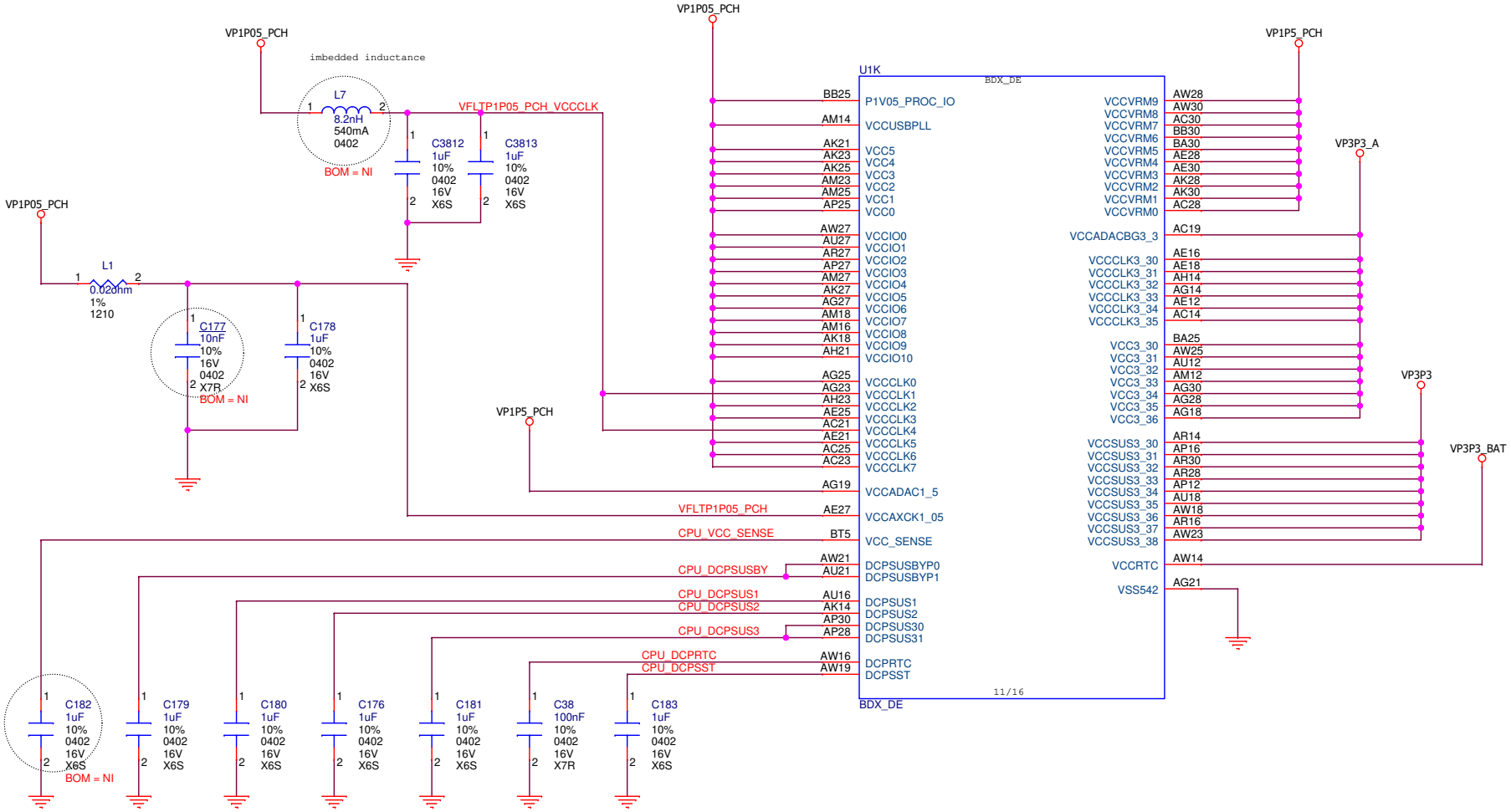
UfiSpace Co., Ltd.

Title: 15. CPU FIVR/JTAG/GPIOS

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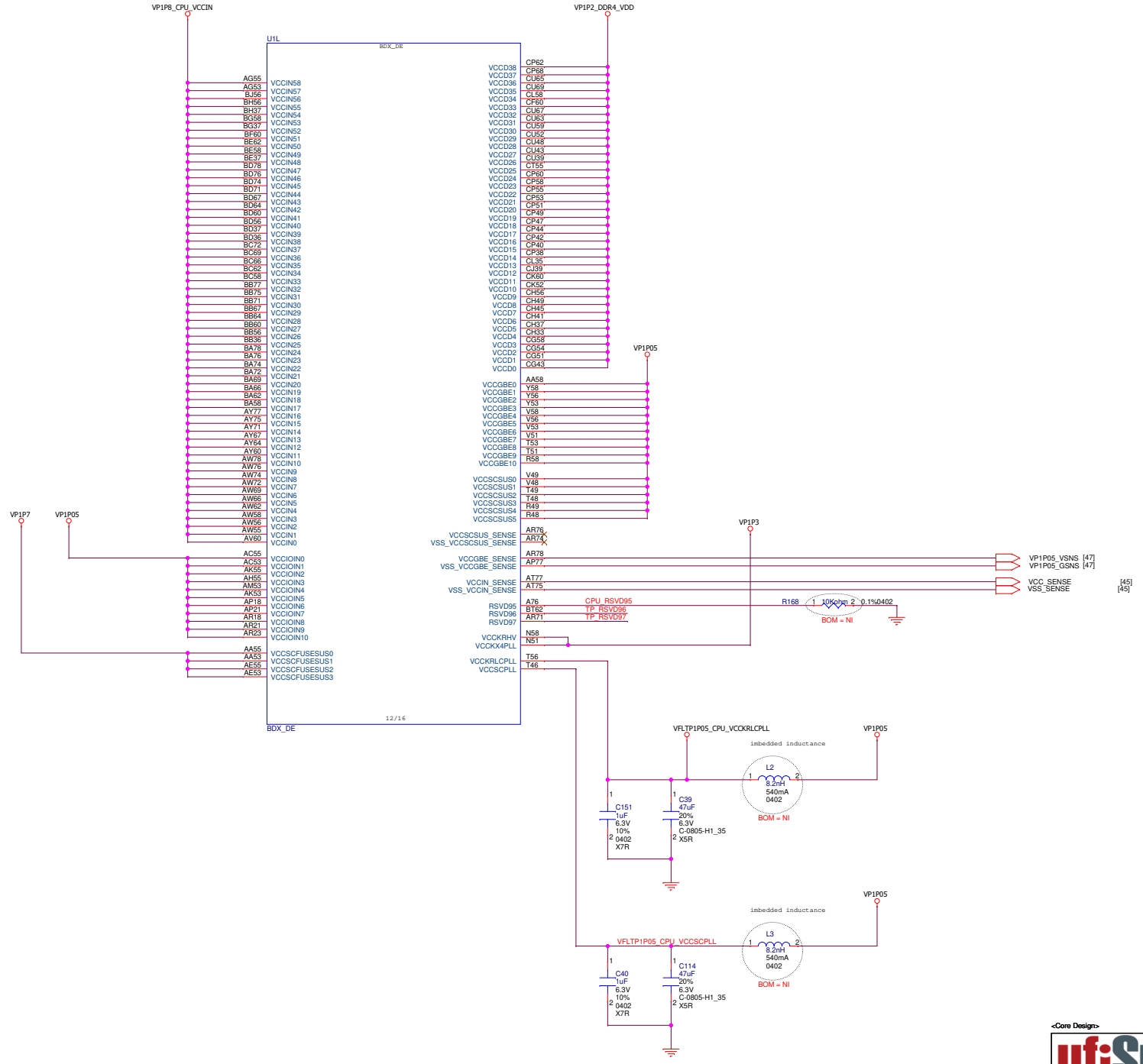
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UfiSpace Co., Ltd.

Title

16. CPU POWER (1/2)

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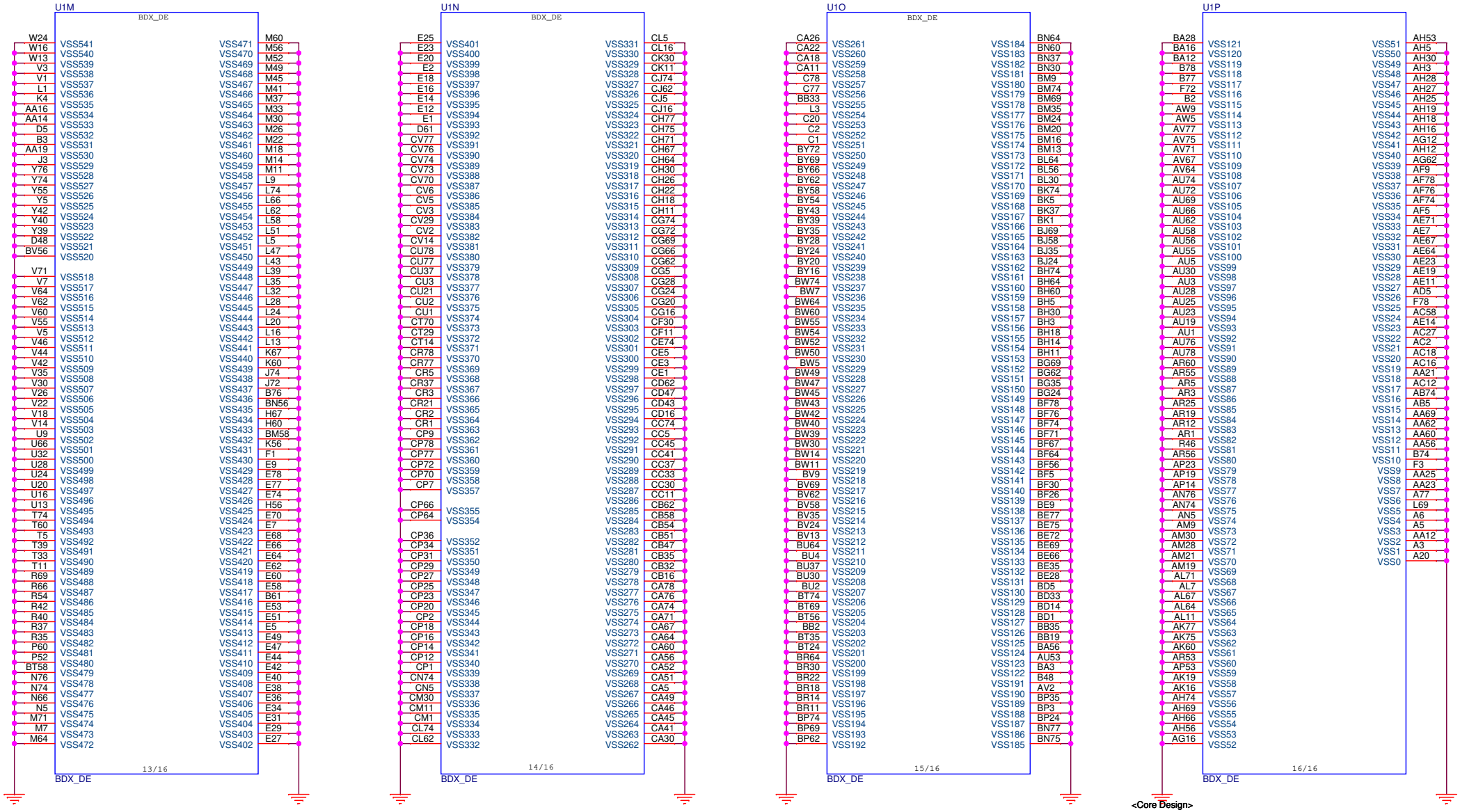
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Title

17. CPU POWER (2/2)

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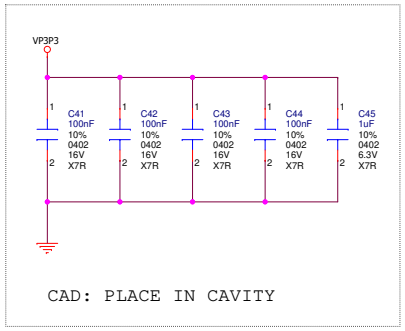
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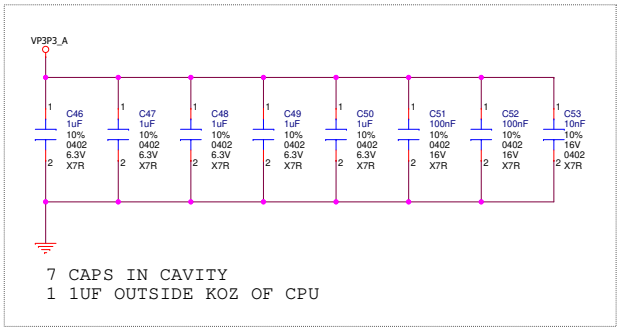
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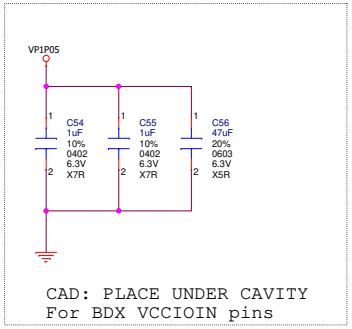
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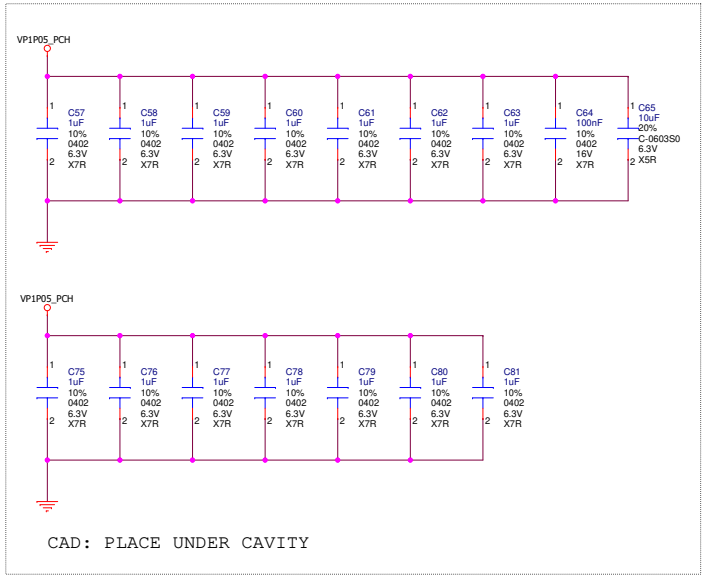
18. CPU GND

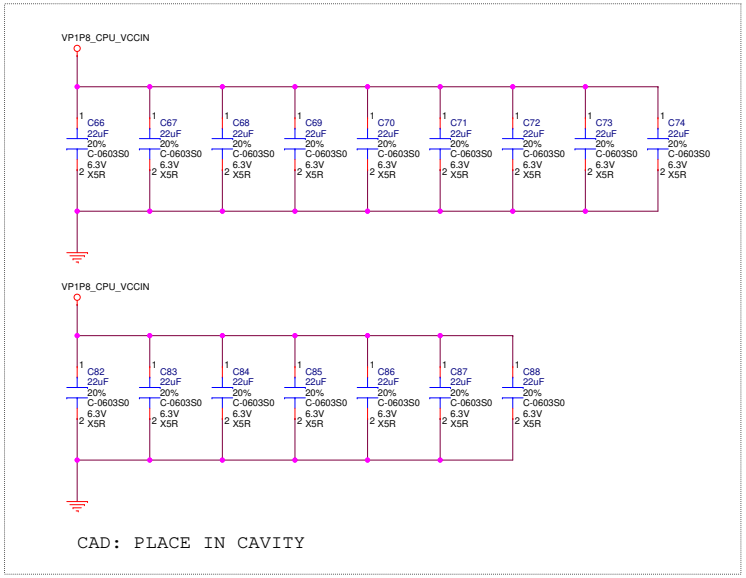
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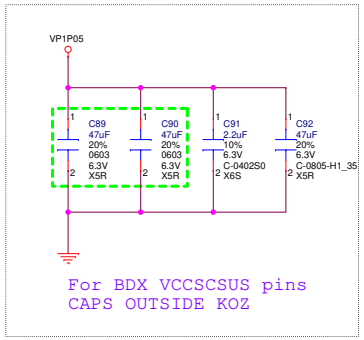


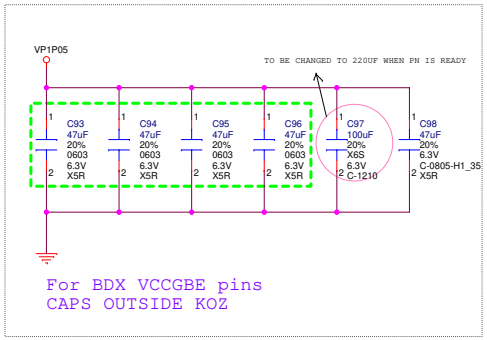


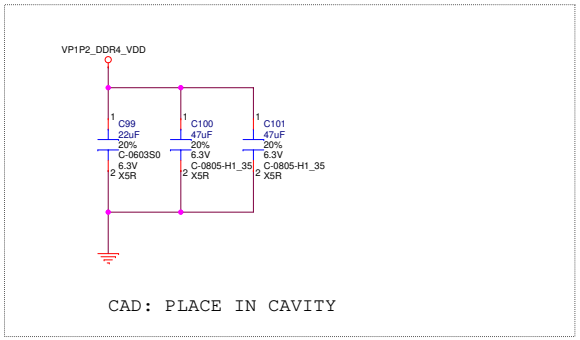












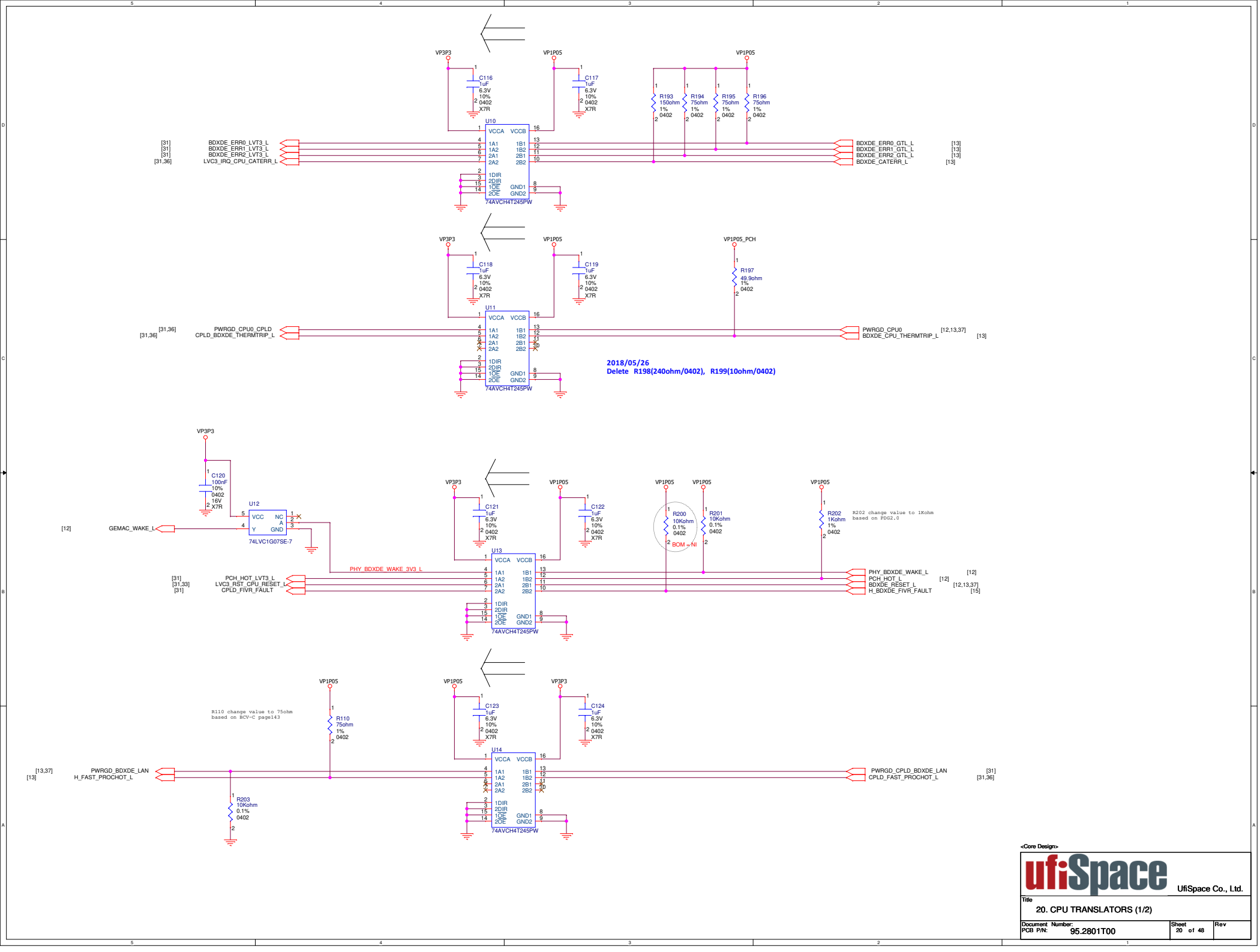
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UfiSpace Co., Ltd.

Title

19. CPU DECOUPLING

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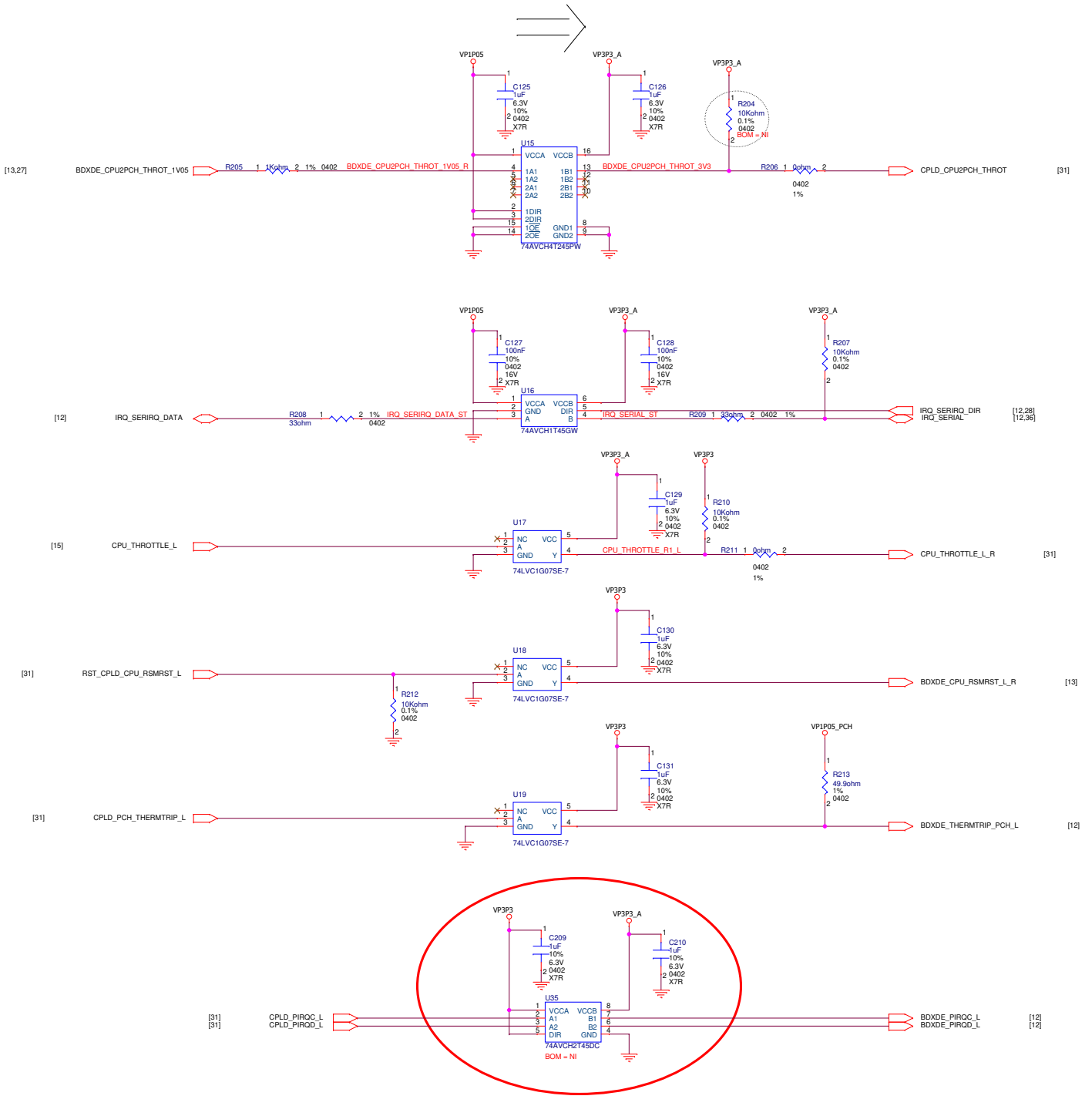
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UfiSpace Co., Ltd.

Title

20. CPU TRANSLATORS (1/2)

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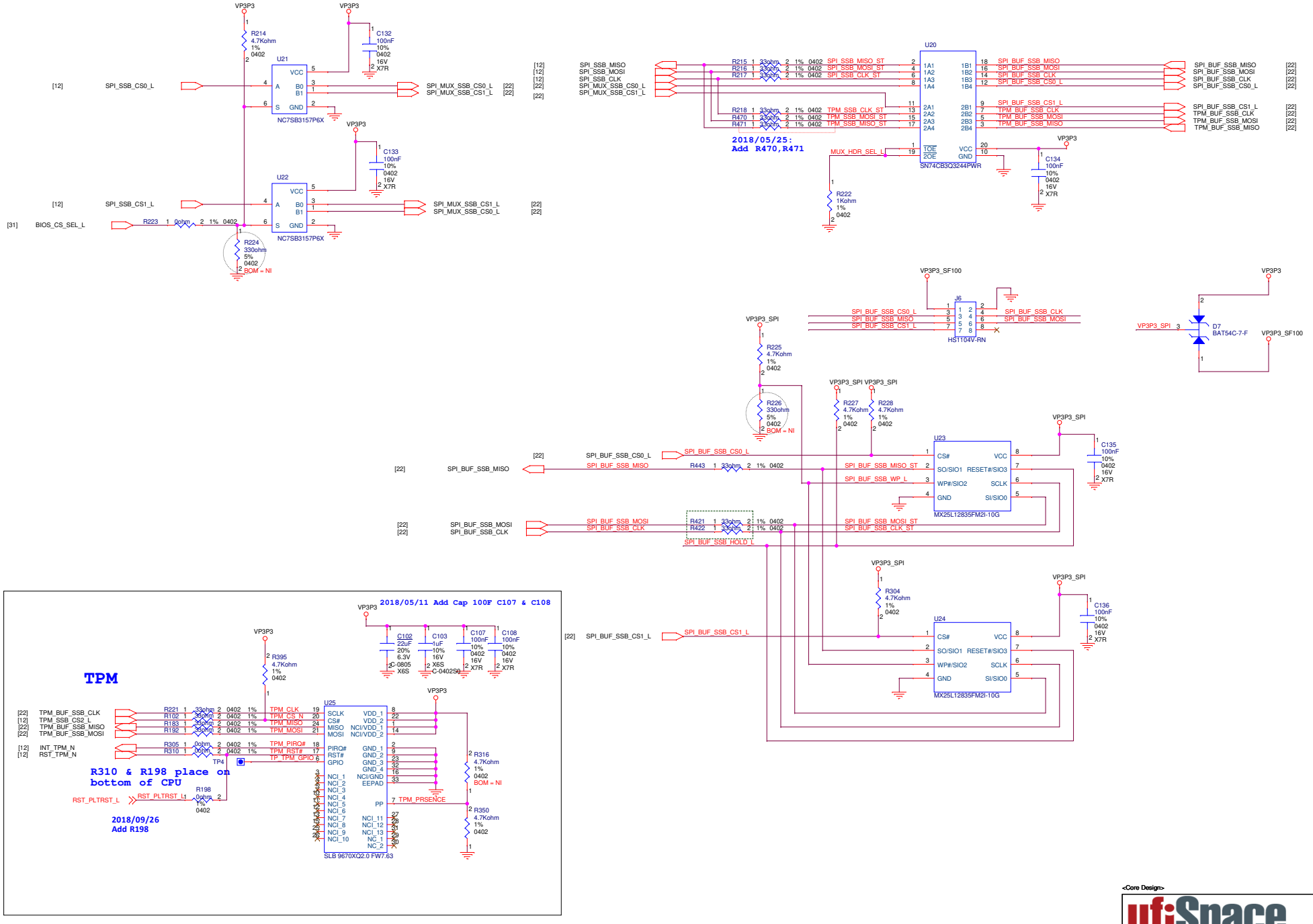
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UfiSpace Co., Ltd.

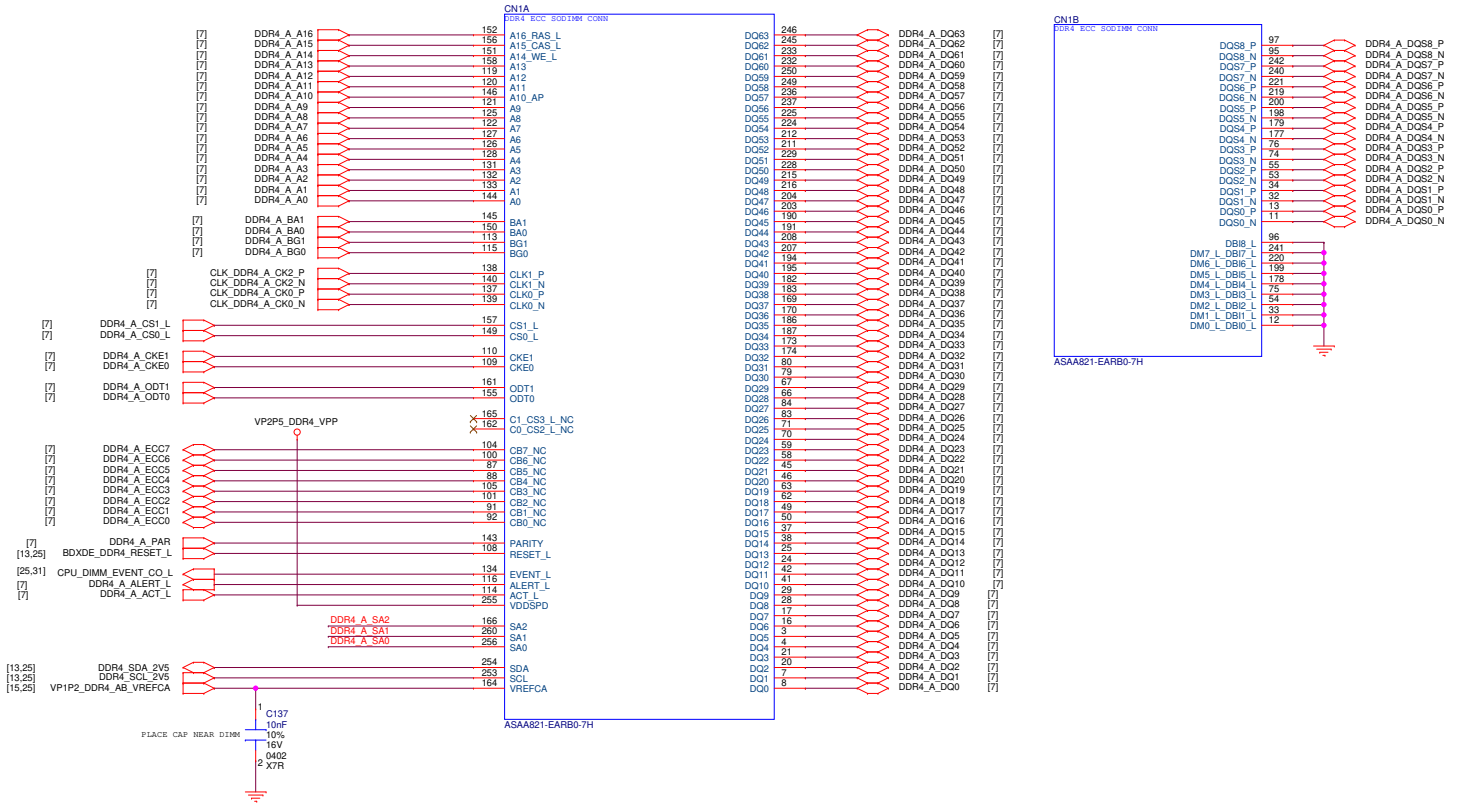
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21. CPU TRANSLATORS (2/2)

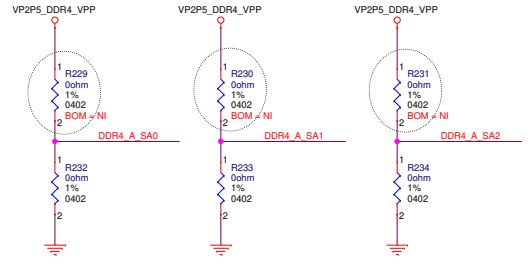
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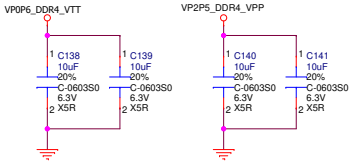

VP3P3
R214 4.7Kohm 1% 0402
C132 100nF 10% 0402 16V X7R
U21
VCC
A B0 B1
S GND
NC7SB3157P6X
[12] SPI_SSB_CS0_L
SPI_MUX_SSB_CS0_L [22]
SPI_MUX_SSB_CS1_L [22]
C133 100nF 10% 0402 16V X7R
U22
[12] SPI_SSB_CS1_L
SPI_MUX_SSB_CS1_L [22]
SPI_MUX_SSB_CS0_L [22]
[31] BIOS_CS_SEL_L
R223 0ohm 1% 0402
R224 330ohm 5% 0402 BOM = NI
[12] SPI_SSB_MISO
[12] SPI_SSB_MOSI
[12] SPI_SSB_CLK
SPI_MUX_SSB_CS0_L [22]
SPI_MUX_SSB_CS1_L [22]
U20
R215 33ohm 1% 0402 SPI_SSB_MISO_ST
R216 33ohm 1% 0402 SPI_SSB_MOSI_ST
R217 33ohm 1% 0402 SPI_SSB_CLK_ST
R218 33ohm 1% 0402 TPM_SSB_CLK_ST
R470 33ohm 1% 0402 TPM_SSB_MOSI_ST
R471 33ohm 1% 0402 TPM_SSB_MISO_ST
SPI_BUF_SSB_MISO [22]
SPI_BUF_SSB_MOSI [22]
SPI_BUF_SSB_CLK [22]
SPI_BUF_SSB_CS0_L [22]
SPI_BUF_SSB_CS1_L [22]
TPM_BUF_SSB_CLK [22]
TPM_BUF_SSB_MOSI [22]
TPM_BUF_SSB_MISO [22]
2018/05/25:
Add R470,R471
MUX_HDR_SEL_L
1OE 2OE VCC GND
SN74CB3Q3244PWR
R222 1Kohm 1% 0402
C134 100nF 10% 0402 16V X7R
VP3P3_SF100
J6
SPI_BUF_SSB_CS0_L
SPI_BUF_SSB_MISO
SPI_BUF_SSB_CS1_L
SPI_BUF_SSB_CLK
SPI_BUF_SSB_MOSI
HST104V-RN
D7 BAT54C-7-F
VP3P3_SPI
R225 4.7Kohm 1% 0402
R226 330ohm 5% 0402 BOM = NI
R227 4.7Kohm 1% 0402
R228 4.7Kohm 1% 0402
U23
CS# VCC
SO/SIO1 RESET#/SIO3
WP#/SIO2 SCLK
GND SI/SIO0
MX25L12835FM2I-10G
C135 100nF 10% 0402 16V X7R
[22] SPI_BUF_SSB_CS0_L
[22] SPI_BUF_SSB_MISO
R443 33ohm 1% 0402
SPI_BUF_SSB_MISO_ST
SPI_BUF_SSB_WP_L
[22] SPI_BUF_SSB_MOSI
[22] SPI_BUF_SSB_CLK
R421 33ohm 1% 0402
R422 33ohm 1% 0402
SPI_BUF_SSB_MOSI_ST
SPI_BUF_SSB_CLK_ST
SPI_BUF_SSB_HOLD_L
R304 4.7Kohm 1% 0402
U24
C136 100nF 10% 0402 16V X7R
[22] SPI_BUF_SSB_CS1_L
TPM
2018/05/11 Add Cap 100F C107 & C108
C102 22uF 20% 6.3V C-0805 X6S
C103 1uF 10% 16V C-0402S6 X6S
C107 100nF 10% 0402 16V X7R
C108 100nF 10% 0402 16V X7R
R395 4.7Kohm 1% 0402
[22] TPM_BUF_SSB_CLK
[12] TPM_SSB_CS2_L
[22] TPM_BUF_SSB_MISO
[22] TPM_BUF_SSB_MOSI
R221 33ohm 1% 0402 TPM_CLK
R102 33ohm 1% 0402 TPM_CS_N
R183 33ohm 1% 0402 TPM_MISO
R192 33ohm 1% 0402 TPM_MOSI
[12] INT_TPM_N
[12] RST_TPM_N
R305 0ohm 1% 0402 TPM_PIRQ#
R310 0ohm 1% 0402 TPM_RST#
TP4 TP_TPM_GPIO
U25
SCLK CS# MISO MOSI
PIRQ# RST# GPIO
VDD_1 VDD_2 NCI/VDD_1 NCI/VDD_2
GND_1 GND_2 GND_3 GND_4 NCI/GND EEPAD
NCI_1 NCI_2 NCI_3 NCI_4 NCI_5 NCI_6 NCI_7 NCI_8 NCI_9 NCI_10
PP
NCI_11 NCI_12 NCI_13 NC_1 NC_2
SLB 9670XQ2.0 FW7.63
R316 4.7Kohm 1% 0402 BOM = NI
TPM_PRSENCE
R350 4.7Kohm 1% 0402
R310 & R198 place on bottom of CPU
R198 0ohm 1% 0402
RST_PLTRST_L
RST_PLTRST_L1
2018/09/26
Add R198
<Core Design>
ufiSpace
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Title
22. CPU BIOS SPI FLASH/TPM
Document Number:
PCB P/N: 95.2801T00
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DDR4 CHA SOCKET



I2C Address = 0xA0 (DIMM0) Channel A
I2C Address = 0xA4 (DIMM1) Channel B





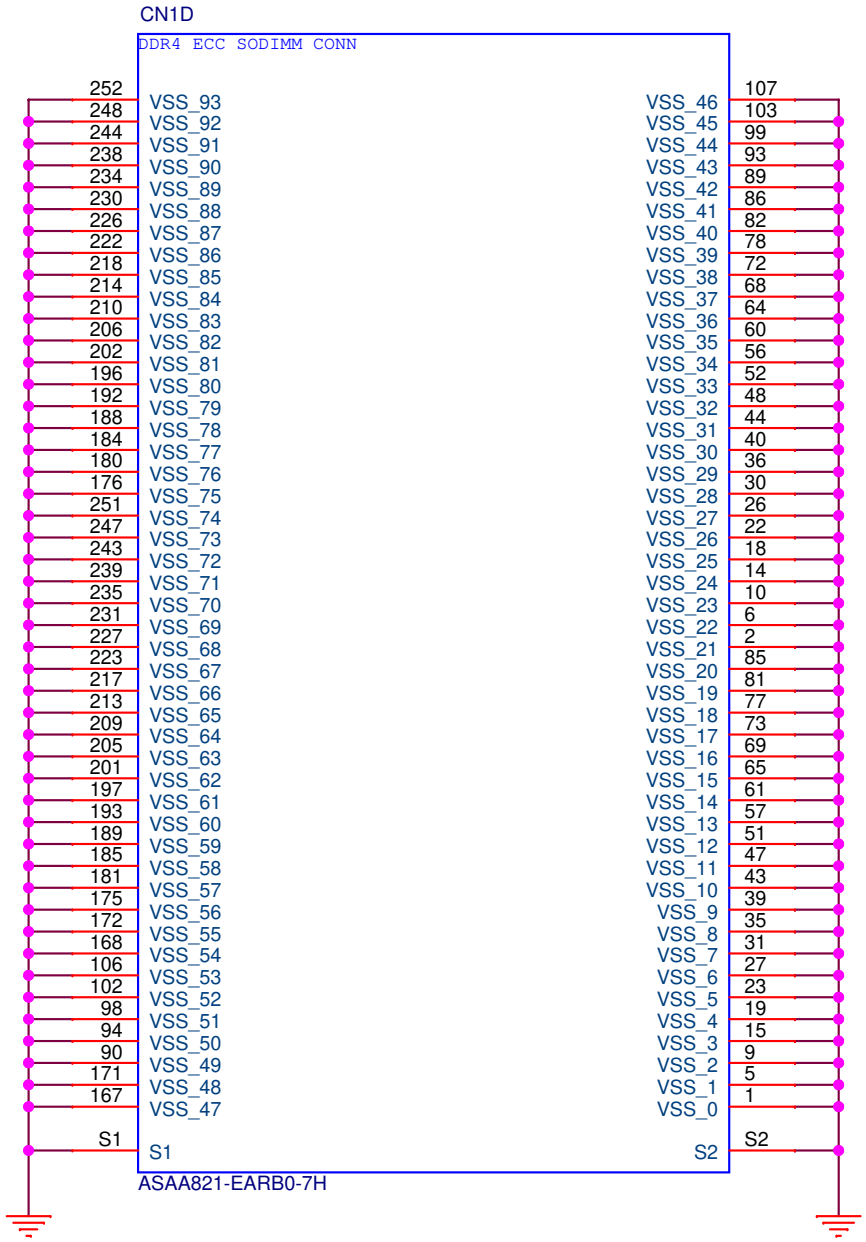
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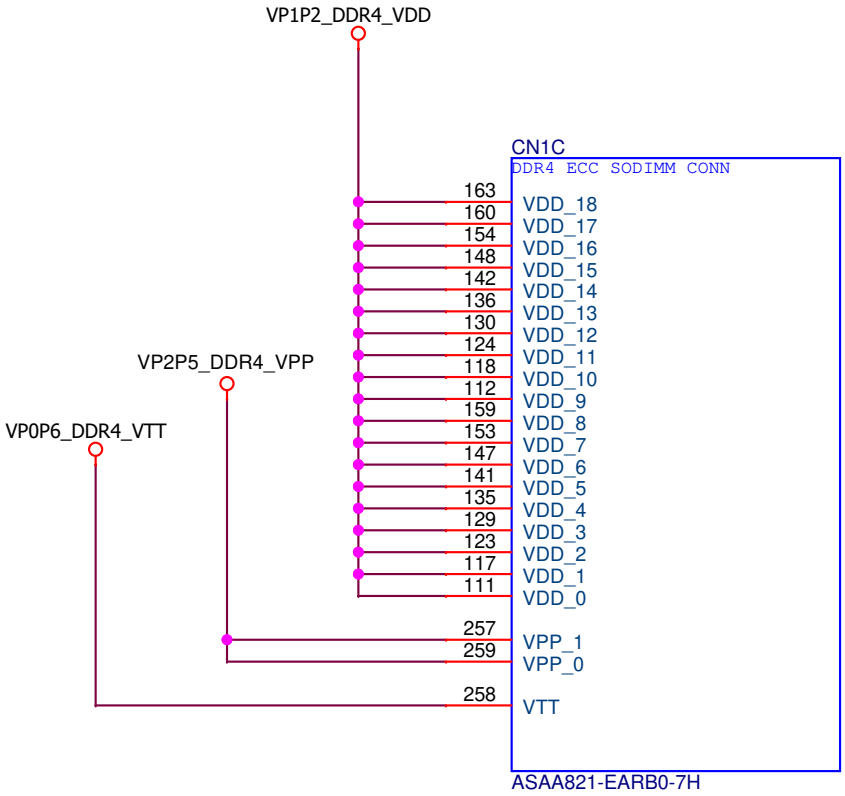
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Title: 23. DDR4 CHA SOCKET

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DDR4 CHA SOCKET PWR





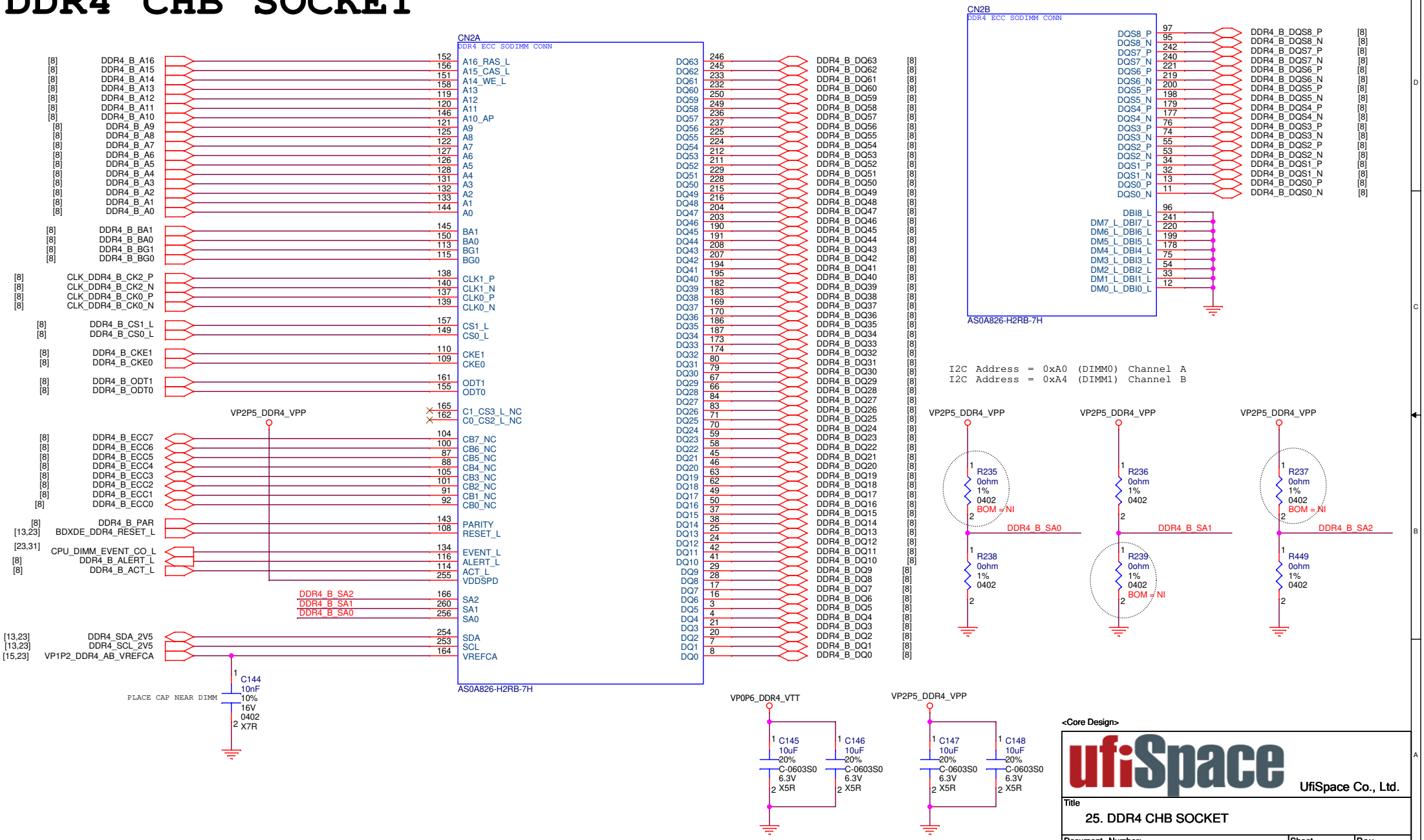
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Title: 24. DDR4 CHA SOCKET PWR

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DDR4 CHB SOCKET



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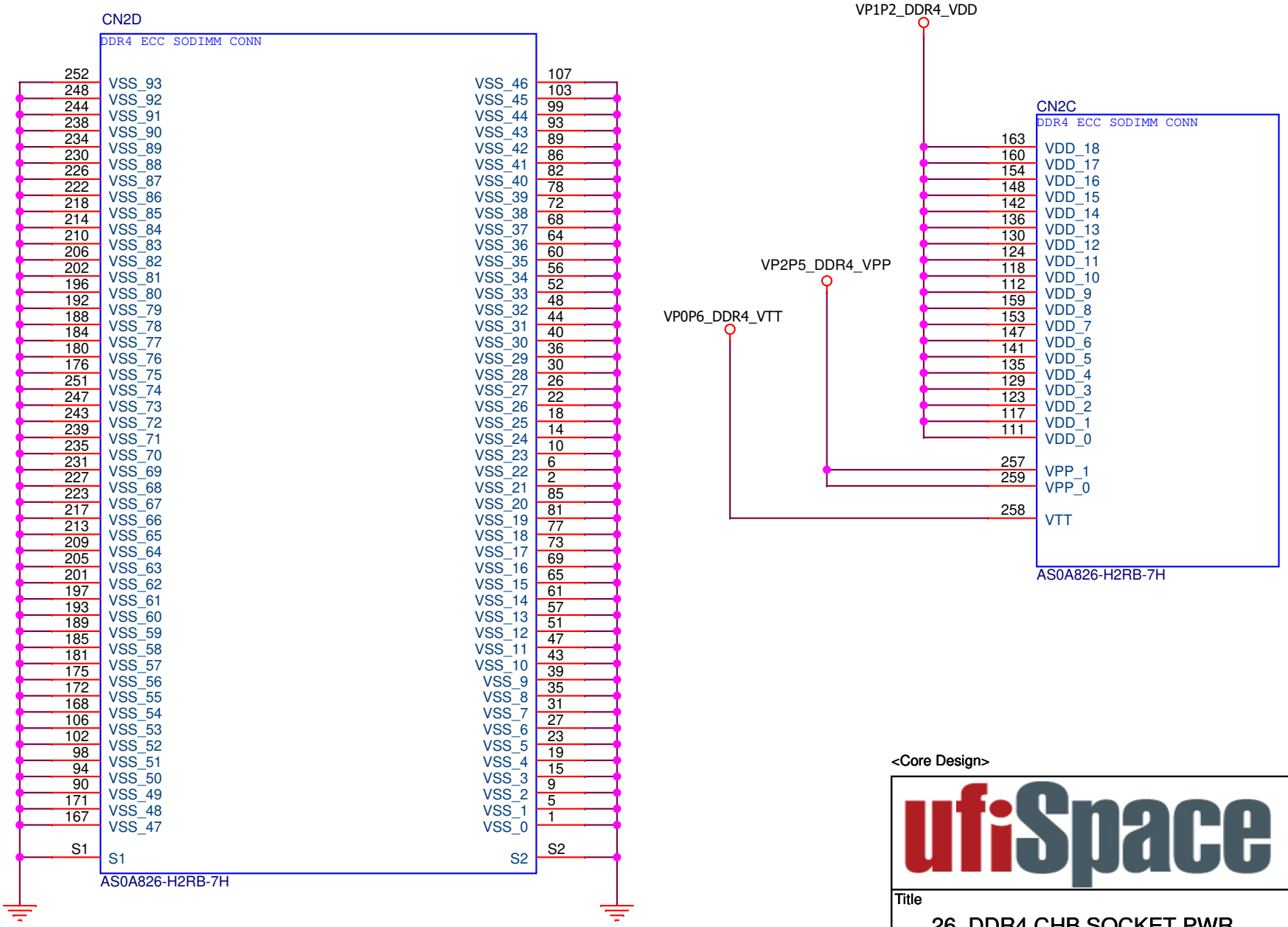
Title: 25. DDR4 CHB SOCKET

Document Number: 95.2801T00

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Rev

DDR4 CHB SOCKET PWR



<Core Design>

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Title

26. DDR4 CHB SOCKET PWR

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GP51_GSXDOUT

VP3P3_A

R240 10Kohm 0402 0.1%

R244 1Kohm 0402 1%

BOM = NI

PU_GPIO51_GSXDOUT [12]

1

BOOT BIOS STRAPS (BBS)		
GNT[51]_GSXDOUT BBS[1]	SATA1GP_GP19 BBS[0]	
0	0	LPC
0	1	NAND
1	0	PCI
1	1	SPI (Default)

SATA1GP_GP19

VP3P3_A

R241 10Kohm 0402 0.1%

R245 1Kohm 0402 1%

BOM = NI

RST_PCIE_PCH_N_GPIO19 [15]

1

DOCKEN_N

VP3P3_A

R242 1Kohm 0402 1%

R246 10Kohm 0402 0.1%

BOM = NI

PD_DMI_TERMINATION_GPIO33 [12]

0

DMI RX TERMINATION WHEN AC-COUPLED MODE:
0 = DMI RX IS TERMINATED TO VSS.(DEFAULT)
1 = DMI RX IS TERMINATED TO VCC/2.

GP53_GSXDIN

VP3P3_A

R243 10Kohm 0402 0.1%

R247 1Kohm 0402 1%

BOM = NI

PD_GPIO53_GSXDIN [12]

0

DMI AC OR DC COUPLEING MODE
0 = DMI IS IN AC-COUPLING MODE
1 = DMI IS IN DC-COUPLING MODE

BIOS_ADV_FUNCTION

VP3P3_A

R248 1Kohm 0402 1%

R253 10Kohm 0402 0.1%

BOM = NI

BIOS_ADV_FUNCTIONS_GPIO36 [15]

0

THIS SIGNAL HAS A WEAK INTERNAL PULL-DOWN.
THIS SIGNAL ONLY TAKES EFFECT IF DMI IS CONFIGURED IN DCCOUPLED MODE
0 = DMI TX IS TERMINATED TO VSS.(DEFAULT)
1 = DMI TX IS TERMINATED TO VCC/2.

ADR_TRIGGER

SATA3 GP37

VP3P3_A

R249 1Kohm 0402 1%

R254 10Kohm 0402 0.1%

BOM = NI

ADR_TRIGGER_L_GPIO37 [15]

1

TLS CONFIDENTIALITY
0 = DISABLE INTEL ME CRPTO TRANSPORT LAYER SECURITY (TLS) CIPHTER SUITE (NO CONFIDENTIALITY)
1 = ENABLE INTEL ME CRPTO TRANSPORT LAYER SECURITY (TLS) CIPHTER SUITE (WITH CONFIDENTIALITY)(DEFAULT)

SUSCLK

GP62

VP3P3

R250 10Kohm 0402 0.1%

R255 1Kohm 0402 1%

BOM = NI

CLK_M2_SUSCLK_ST [12]

1

PLL ON-DIE VOLTAGE REGULATOR ENABLE.
1 = ENABLED
0 = DDISABLED
WEAK INTERNAL PU (15K-40K).

NCSI_TRI_EN

VP1P05

R251 5.11Kohm 1% 0402

R256 5.11Kohm 1% 0402

BOM = NI

LAN_NCSI_TRI_EN_L [10]

0

CPU2PCH_THROT

VP1P05

R252 5.11Kohm 1% 0402

R257 5.11Kohm 1% 0402

BOM = NI

BDXDE_CPU2PCH_THROT_1V05 [13,21]

0

SPARE[0]

VP1P05

R258 5.11Kohm 1% 0402

R263 5.11Kohm 1% 0402

BOM = NI

BDXDE_PECID0 [13]

0

PECI_ID[2:0]=000B

SPARE[1]

VP1P05

R259 5.11Kohm 1% 0402

R264 5.11Kohm 1% 0402

BOM = NI

PD_BDXDE_SPARE1 [13]

0

THIS IS THE DISABLE TO THE SC PCU RESET FSM
0 = PMC FSB BRINGS UP SOUTH COMPLEX
1 = PCODE BRINGS UP SOUTH COMPLEX OF PMC

SPARE[2]

VP1P05

R260 5.11Kohm 1% 0402

R265 5.11Kohm 1% 0402

BOM = NI

PD_BDXDE_SPARE2 [13]

0

BYPASSES THE CRYSTAL CLOCK TO THE SCPLL
1'B0 = PICKS THE 25MHZ KR CRYSTAL CLOCK AS THE REFERENCE TO SCPLL (DEDAULT)
1'B1 = FORCES THE TEST DOCK FROM TSTCLK_SC PINS

SPARE[3]

VP1P05

R261 5.11Kohm 1% 0402

R266 5.11Kohm 1% 0402

BOM = NI

PD_BDXDE_SPARE3 [13]

0

SELECTS B/W FUNCTIONAL AND TEST MODE IN THE KX4 PLL
1'B0 = NO TEST CLOCK OVERRIDE (DEFAULT)
1'B1 = TEST CLOCK OVERRIDE

SPARE[4]

VP1P05

R262 5.11Kohm 1% 0402

R267 5.11Kohm 1% 0402

BOM = NI

PD_BDXDE_SPARE4 [13]

0

1'B0 = NORMAL REFERENCE CLOCK PATH WITH CR BASE REFERENCE CLOCK SELECTION(DEFAULT)
1'B1 = FORCE "REGULAR" REFERENCE CLOCKS TO BE SENT TO THE KX4 PLLS AS LONG AS TSTCLK_KX4_STRAP[2]=1'B0

UART_TXD[0]

VP1P05

R268 5.11Kohm 1% 0402

R274 5.11Kohm 1% 0402

BOM = NI

CPU_UART0_TXD_1V05 [13]

0

UART_TXD[1]

VP1P05

R269 5.11Kohm 1% 0402

R275 5.11Kohm 1% 0402

BOM = NI

CPU_UART1_TXD_1V05 [13]

0

NCSI_ARB_OUT

VP1P05

R270 5.11Kohm 1% 0402

R276 5.11Kohm 1% 0402

BOM = NI

LVC1_LAN_NCSI_ARB_OUT [10]

1

SELECTS B/W THE COMBINED AND SEPERATE VRS
1: USING COMBINED P1V05 VR (DEFAULT)
0: ALL RAILS HAVE SEPERATE VRS

DSWODVREN

VP3P3_BAT

R271 5.11Kohm 1% 0402

PU_DSWODVREN [12]

1

DSWODVREN: DEEP SLEEP WELL ON-DIE VOLTAGE REGULATOR ENABLE
1: DSW ODVR IS ENABLED (DEFAULT).
0: DSW ODVR IS DISABLED.

NCSI_RXD_1

VP1P05

R272 5.11Kohm 1% 0402

R277 5.11Kohm 1% 0402

BOM = NI

LAN_NCSI_RXD1 [10]

0

ENABLE/DISABLE MANAGEBILITY TRAFFIC
DEFAULT LOW - DISABLED
1'B0 = LAN AVAILABLE IN S5 FOR WOL (DEFAULT)
1'B1 = LAN NOT AVAILABLE IN S5.
MANAGEBILITY DISABLED.
NO ON-DIE PU / PDN

INTVRMEN

VP3P3_BAT

R273 330Kohm 1% 0402

PU_BDXDE_INTVRMEN [12]

1

INTERNAL VRM ENABLE:
THIS SIGNAL IS USED TO ENABLE OR DISABLE THE INTEGRATED 1.05V REGULATOR FOR THE SUSPEND WELL ON THE WBG.
PU: ENABLE VR (DEFAULT).
PD: DISABLES VR..
PD OPTION NOT BEING PROVIDED.

10GBE_MDIO_DIR_CTL_1

VP1P05

R278 5.11Kohm 1% 0402

R283 5.11Kohm 1% 0402

BOM = NI

LAN_10GE_P1_MDIO_DIR_1V05 [10]

1

2'B00 = BOTH LAN PORTS ARE DISABLED.
NOTE: IN THIS MODE MANAGEABILITY IS NOT FUNCTIONAL AND MUST NOT BE ENABLED IN NVM CONTROL WORD 1.
2'B01 = PORT 1 IS DISABLED. PORT 0 IS ENABLED.
2'B10 = RESERVED
2'B11 = BOTH PORT0 & 1 ARE ENABLED.(DEFAULT)

10GBE_MDIO_DIR_CTL_0

VP1P05

R279 5.11Kohm 1% 0402

R284 5.11Kohm 1% 0402

BOM = NI

LAN_10GE_P0_MDIO_DIR_1V05 [10]

1

DDR3_4_STRAP

VP1P05

R280 240ohm 1% 0402

R285 240ohm 1% 0402

BOM = NI

PU_DDR3_4_STRAP [13]

1

SELECTS BETWEEN DDR4 & DDR3:
1 = DDR4
0 = DDR3

TXT_PLTEN

TXT_PLTEN [13]

R282 240ohm 1% 0402

BOM = NI

1

PLATFORM ENABLE STRAP.
0 = THE PLATFORM IS NOT INTEL TXT ENABLED.
1 = DEFAULT. THE PLATFORM IS INTEL TXT ENABLED

TXT_AGENT

VP1P05

R281 240ohm 1% 0402

R286 240ohm 1% 0402

BOM = NI

TXT_AGENT [13]

1

TXT AGENT (DRIVES TXT TRANSANCTIONS):
1 = CPU IS TXT_AGENT
0 = CPU IS NOT TXT_AGENT

<Core Design>

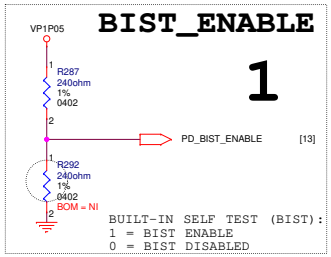
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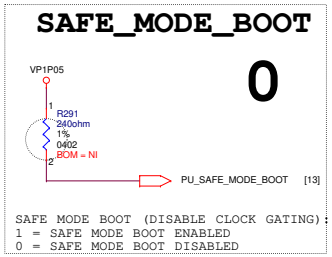
Title: 27. CPU STRAPS (1/2)

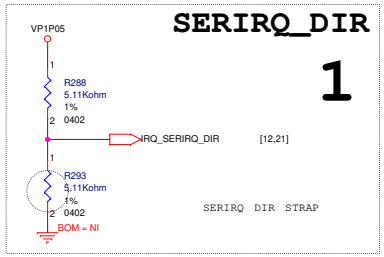
Document Number: PCB P/N: 95.2801T00

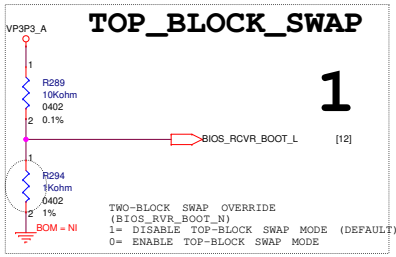
Sheet 27 of 48

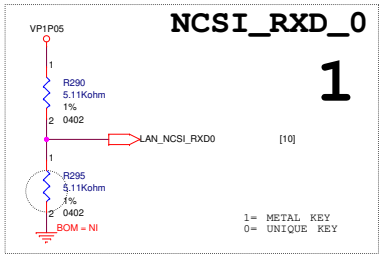
Rev

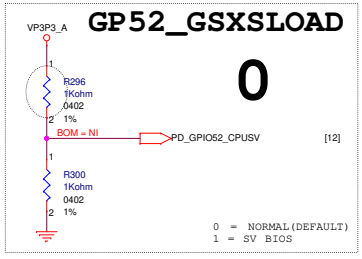


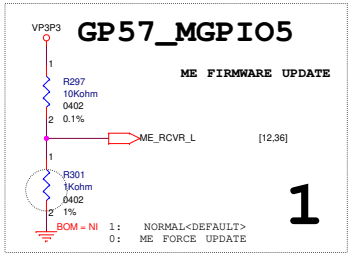


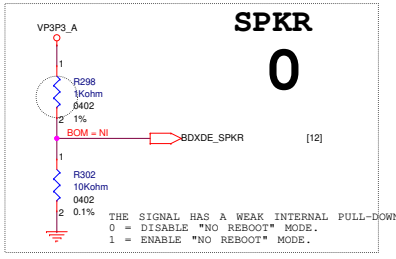


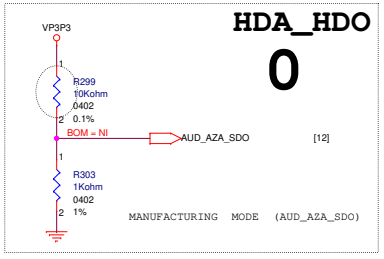












STRAP_NAME	DEFAULT	DESCRIPTION
BOOT BIOS STRAPS (GP19, GP51)	1,1	BOOT BIOS DESTINATION 0 1 RESERVED 1 0 RESERVED 1 1 SPI (DEFAULT) 0 0 LPC
DMI_TERMINATION	0	DMI TX TERMINATION WHEN DCCOUPLED MODE. 0 = DMI TX IS TERMINATED TO VSS. 1 = DMI TX IS TERMINATED TO VCC/2.
BIOS_ADV_FUNCTIONS	0	DMI RX TERMINATION WHEN AC-COUPLED MODE: 0 = DMI RX IS TERMINATED TO VSS.(DEFAULT) 1 = DMI RX IS TERMINATED TO VCC/2.
GSXDIN	0	DMI AC OR DC COUPLING? 0 = DMI IS IN AC-COUPLING MODE (SERVER/WORKSTATION ONLY, NOT MEANT FOR DESKTOP/MOBILE) 1 = DMI IS IN DC-COUPLING MODE (DESKTOP, MOBILE OR SERVER/WORKSTATION).
ADR_TRIGGER	1	TLS CONFIDENTIALITY 0 = DISABLE INTEL ME CRYPTO TRANSPORT LAYER SECURITY (TLS) 1 = ENABLE INTEL ME CRYPTO TRANSPORT LAYER SECURITY (TLS)
SUSCLK	1	TLS CONFIDENTIALITY 0 = DISABLE INTEL ME CRYPTO TRANSPORT LAYER SECURITY (TLS) 1 = ENABLE INTEL ME CRYPTO TRANSPORT LAYER SECURITY (TLS)
NCSI_TRI_EN CPU2PCH_THROT SPARE[0]	0,0,0	STRAPS HERE TO IDENTIFY WHICH SOCKET IS WHICH IN ORDER FOR PECI TO WORK
SPARE[1]	0	THIS IS THE DISABLE TO THE SC PCU RESET FSM 0 = PMC FSB BRINGS UP SOUTH COMPLEX 1 = PCODE BRINGS UP SOUTH COMPLEX OF PMC
SPARE[2]	0	BYPASSES THE CRYSTAL CLOCK TO THE SCPLL 0 = PICKS THE 25MHZ KR CRYSTAL CLOCK AS THE REFERENCE TO SCPLL (DEFAULT) 1 = FORCES THE TEST CLOCK FROM TSTCLK_SC PINS
SPARE[3]	0	SELECTS B/W FUNCTIONAL AND TEST MODE IN THE KX4 PLL 0 = NO TEST CLOCK OVERRIDE (DEFAULT) 1 = TEST CLOCK OVERRIDE
SPARE[4]	0	SELECTS B/W FUNCTIONAL AND TEST MODE IN THE KX4 PLL 0 = NORMAL REFERENCE CLOCK PATH WITH CR BASED REFERENCE CLOCK SELECTION (DEFAULT) 1 = FORCE "REGULAR" REFERENCE CLOCKS TO BE SENT TO THE KX4 PLLS
UART_TXD[0]	0	JTAG PORT FOR NORTH COMPLEX TAP 0 = GB#_SDP* PINS ARE USED AS FUNCTIONAL PIN OR CAN BE USED FOR SC TAPS THROUGH TAP PROGRAMMING. (DEFAULT) 1 = PINS ARE USED AS JTAG PORT FOR NC TAP
UART_TXD[1]	0	CONTROLS THE SECURITY ATTRIBUTES ON THE NVM – FOR PRE- PRODUCTI ON USAGE 0 = DISABLES NVM SECURITY (DEFAULT) 1 = SECURITY ENABLED

STRAP_NAME	DEFAULT	DESCRIPTION
NCSI_ARB_OUT	1	USING COMBINED P1V05
DSWODVREN	1	0 = DISABLE INTEGRATED DEEPSX WELL (DSW) ON-DIE VOLTAGE REGULATOR. THIS MODE IS ONLY SUPPORTED FOR TESTING ENVIRONMENTS. 1 = ENABLE DSW 3.3V-TO-1.05V INTEGRATED DEEPSX WELL (DSW) ON-DIE VOLTAGE REGULATOR.
NCSI_RXD_1	0	ENABLE/DISABLE MANAGEBILITY TRAFFIC 0 = LAN AVAILABLE IN S5 FOR WOL (DEFAULT) 1 = LAN NOT AVAILABLE IN S5. MANAGEBILITY DISABLED.
INTVRMEN	1	INTEGRATED VRMS 0 = DCPSUS1, DCPSUS2 AND DCPSUS3 ARE POWERED FROM AN EXTERNAL POWER SOURCE. SERVERS SHOULD NOT PULL THE STRAP LOW. 1 = INTEGRATED VRMS ENABLED.
10GBE_MDIO_DIR_CTL_0 10GBE_MDIO_DIR_CTL_1	1,1	00 = BOTH LAN PORTS ARE DISABLED. 01 = PORT 1 IS DISABLED. PORT 0 IS ENABLED. 10 = RESERVED 11 = BOTH PORT0 & 1 ARE ENABLED. (DEFAULT)
DDR3_4_STRAP	1	1 = DDR4 0 = DDR3
TXT_PLTEN	1	(INTEL? TXT) PLATFORM ENABLE STRAP. 0 = THE PLATFORM IS NOT INTEL TXT ENABLED. 1 = DEFAULT. THE PLATFORM IS INTEL TXT ENABLED
TXT_AGENT	1	TXT AGENT (DRIVES TXT TRANSANCTIONS): 1 = CPU IS TXT_AGENT 0 = CPU IS NOT TXT_AGENT
BIST_ENABLE	1	BUILT-IN SELF TEST (BIST): 1 = BIST ENABLED 0 = BIST DISABLED
SAFE_MODE_BOOT	0	SAFE MODE BOOT (DISABLE CLOCK GATING): 1 = SAFE MODE BOOT ENABLED 0 = SAFE MODE BOOT DISABLED

<Core Design>

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Title: 28. CPU STRAPS (2/2)

Document Number: PCB P/N: 95.2801T00

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CPU I2C address:
1. 0x4F --Temp sensor:
2. 0x57 -- EEPROM address
3. 0x77 -- PCA9539 IO EXP address
4. 0xA0 -- (DIMM0) Channel A
5. 0xA4 -- (DIMM1) Channel B
6. 0x44 -- SOC legacy SMBus ARP slave address
7. 0x48 -- Diag Service SMBus address
8. 0x08 -- SMBus Host Controller

[15,36,37] SMB_HOST_3V3SB_CLK
[15,36,37] SMB_HOST_3V3SB_DAT

U26 M24128-BRDW6TP
I2C Address : 7b' 101_0111 (0x57)
R317 0ohm 0402 I2C_EEPROM_SCL
R318 0ohm 0402 I2C_EEPROM_SDA
R319 330ohm
R320 330ohm R-0402S0 5% BOM = NI
R321 330ohm R-0402S0 5% BOM = NI
R446 330ohm R-0402S0 5% BOM = NI
R444 4.7Kohm 1% 0402
R445 4.7Kohm 1% 0402
R315 4.7Kohm 1% 0402
C152 100nF 10% 0402 16V X7R

2018/05/15
1.Add pull up/down resistors on EEPROM address pins
2.Change the CPU's EEPROM address from 0x51 to 0x57 to avoid the I2C address conf li ct

[36] ADC_CPU_TEMP_SENSOR

2018/04/17 Add ADC Thermal Sensor

Place close to Broadwell-DE(U1)

U36 TMP235A2DCKR 020.00086.005 SC-70-5A
C105 100nF 10% 0402 16V X7R

U27 TMP75AIDR
I2C Address : 7b' 100_1111 (0x4F)
R322 4.7Kohm 1% 0402
R323 0ohm 0402 I2C_TEMP_SENSOR_SDA
R324 0ohm 0402 I2C_TEMP_SENSOR_SCL
SMB_HOST_3V3SB_ALERT_L [15,29,36]
C153 100nF 10% 0402 16V X7R

2018/05/26
Add C106,C109

C106 100nF 10% 0402 16V X7R
C109 100nF 10% 0402 16V X7R

U28 74LVC1G07SE-7
SMI_ACTIVE_L_R R325 0ohm 0402 SMI_ACTIVE_L_BUF
SMI_ACTIVE_L [15]

U29 74LVC1G07SE-7
NMI_EVENT_L_R R330 0ohm 0402 NMI_EVENT_L_BUF
NMI_EVENT_L [15]

SMI_ACTIVE_L_R R326 4.7Kohm 0402
NMI_EVENT_L_R R327 4.7Kohm 0402
SMI_ACTIVE_L R332 4.7Kohm 0402
NMI_EVENT_L R333 4.7Kohm 0402

U30 PCA9539PW
I2C Address : 7b' 111_0111 (0X77)
R328 0ohm 0402
R329 0ohm 0402
R331 4.7Kohm 1% 0402
R334 4.7Kohm 1% 0402
R335 4.7Kohm 1% 0402
R336 4.7Kohm 1% 0402 BOM = NI
R337 4.7Kohm 1% 0402 BOM = NI
C154 100nF 10% 0402 16V X7R
C155 1uF 10% 0402 16V X6S
[15,29,36] SMB_HOST_3V3SB_ALERT_L
I2C_IO_EXP_SCL
I2C_IO_EXP_SDA

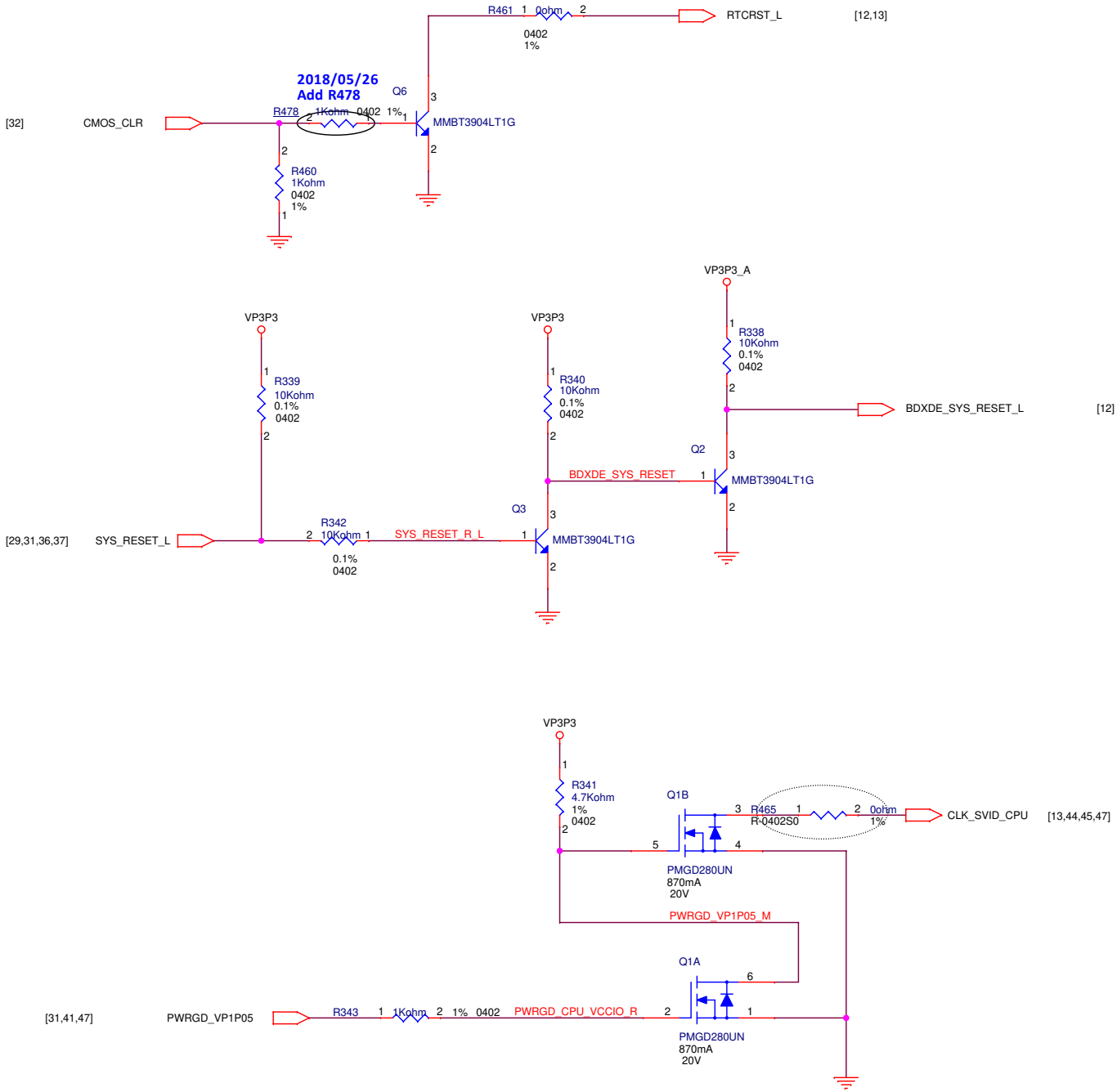
CPLD_ERROR2_L_LATCH	[31]
CPLD_ERROR1_L_LATCH	[31]
CPLD_ERROR0_L_LATCH	[31]
CPLD_CATERR_L_LATCH	[31]
CPLD_PCHHOT_L_LATCH	[31]
CPLD_PROCHOT_L_LATCH	[31]
CPLD_THERMTRIP_L_LATCH	[31]
SYS_PWROK	[12,31,37]
SLP3_L	[12,31]
SYS_RESET_L	[30,31,36,37]
FP_IBMC_PWRBTN_OUT_L	[12,31,36,37]
CPLD_PLTRST_L_LATCH	[31]
SLP4_L	[12,31]
CPLD_CLEAR_LATCH	[31]

<Core Design>

UfiSpace Co., Ltd.

Title: 29. EEPROM/SENSOR/IO EXPANDER

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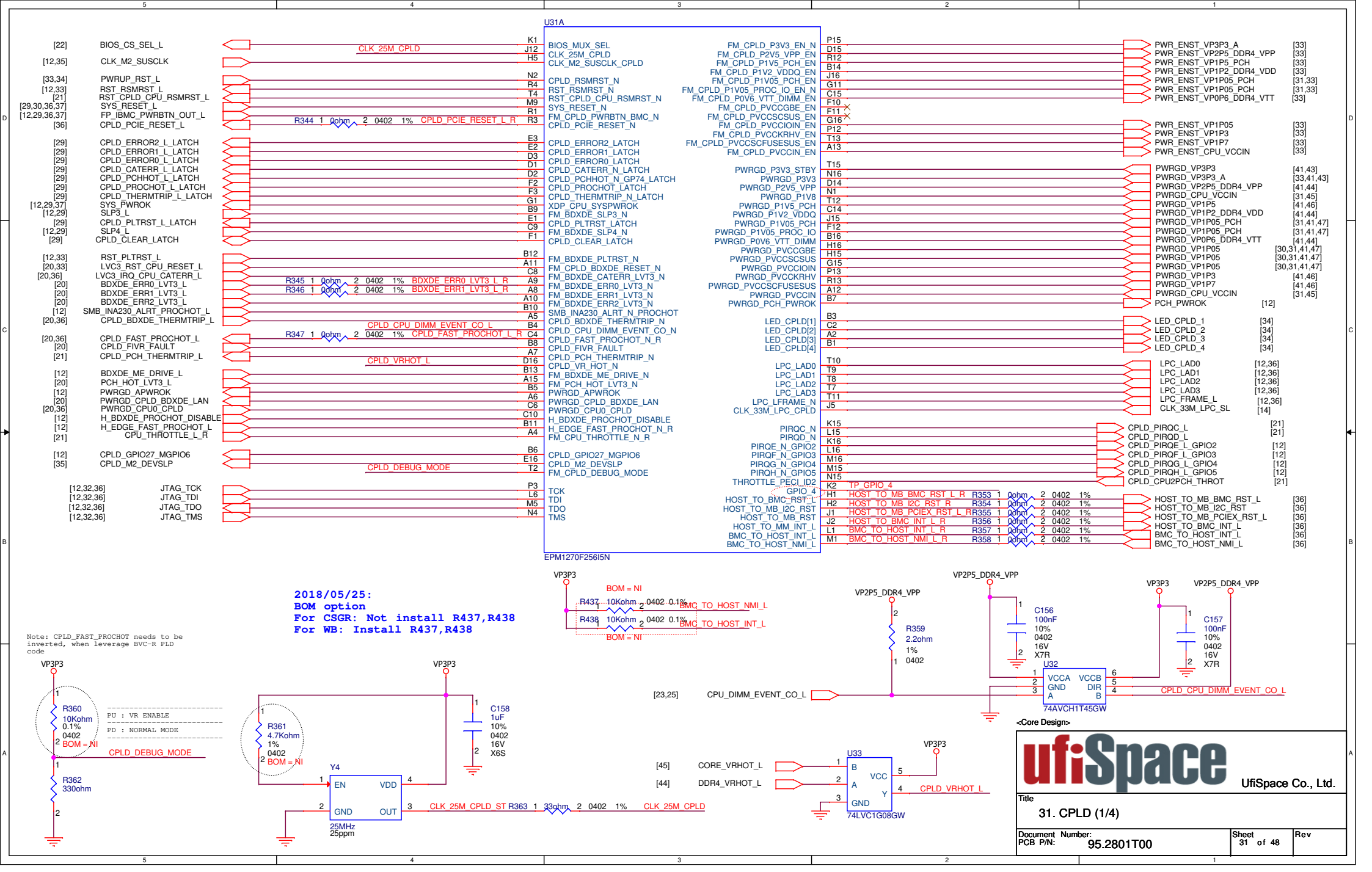
<Core Design>

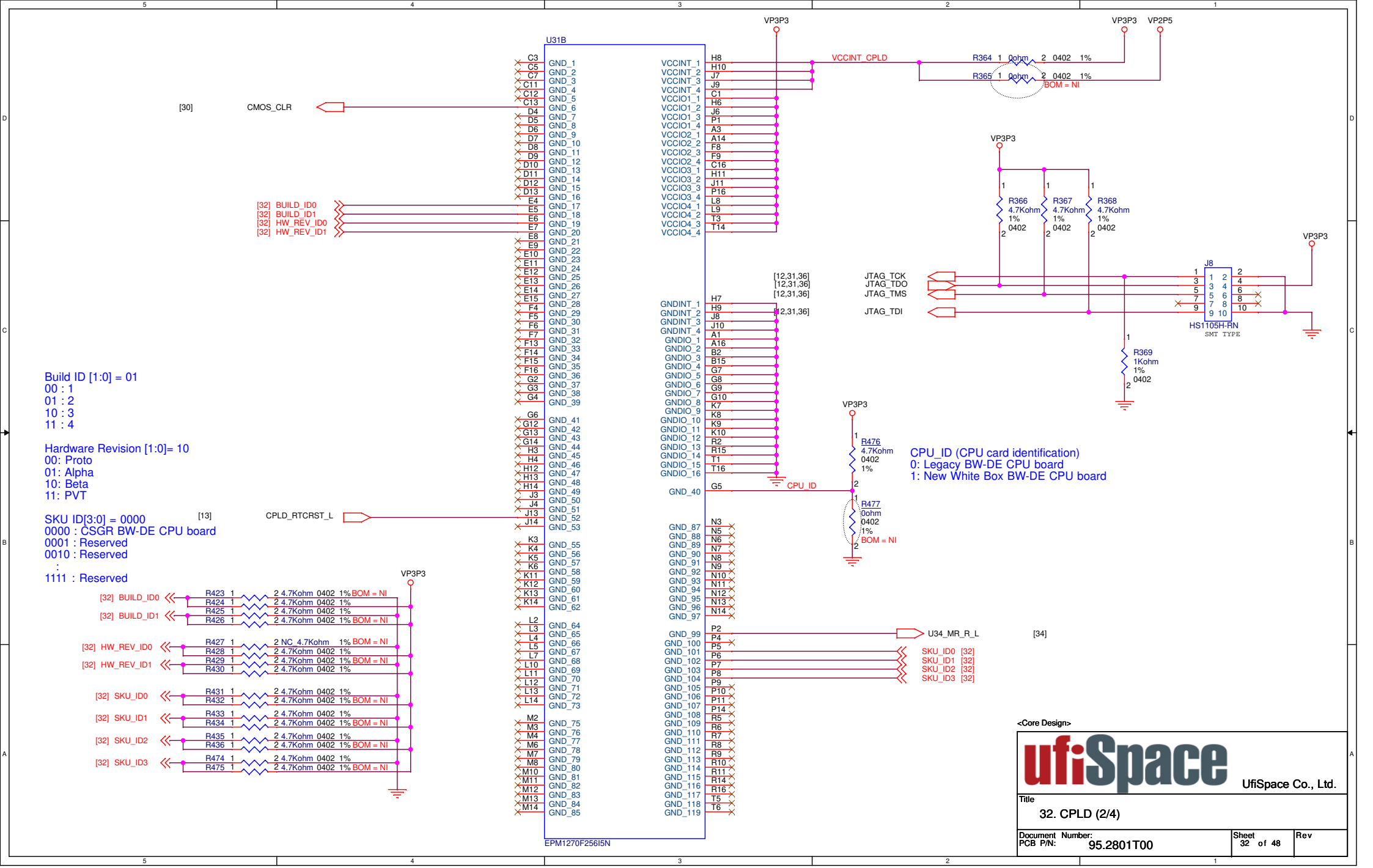
UfiSpace Co., Ltd.

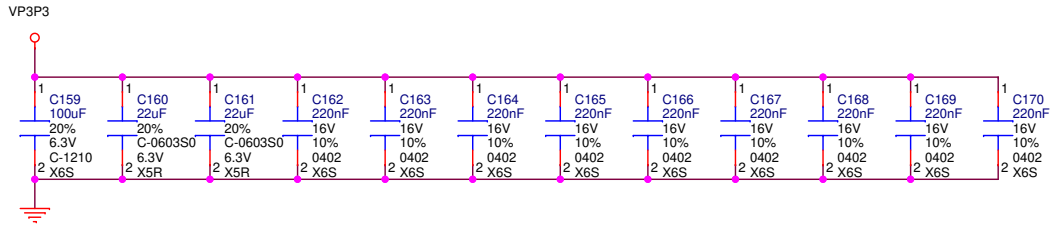
Title

30. CPU MSIC

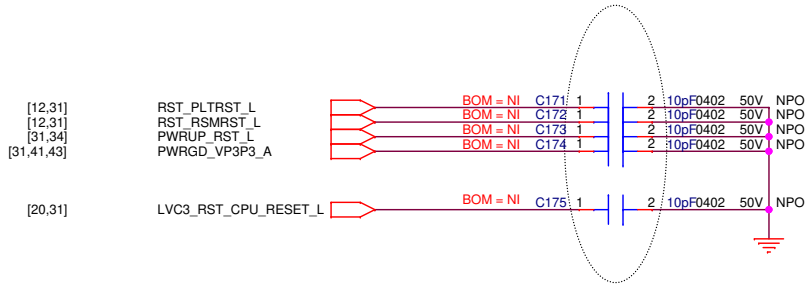
Document Number:	Sheet	Rev
PCB P/N: 95.2801T00	30 of 48	


U31A
EPM1270F256I5N
2018/05/25:
BOM option
For CSGR: Not install R437,R438
For WB: Install R437,R438
Note: CPLD_FAST_PROCHOT needs to be inverted, when leverage BVC-R PLD code
PU : VR ENABLE
PD : NORMAL MODE
74AVCH1T45GW
74LVC1G08GW
25MHz 25ppm
<Core Design>
UfiSpace Co., Ltd.
Title
31. CPLD (1/4)
Document Number: 95.2801T00
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Rev

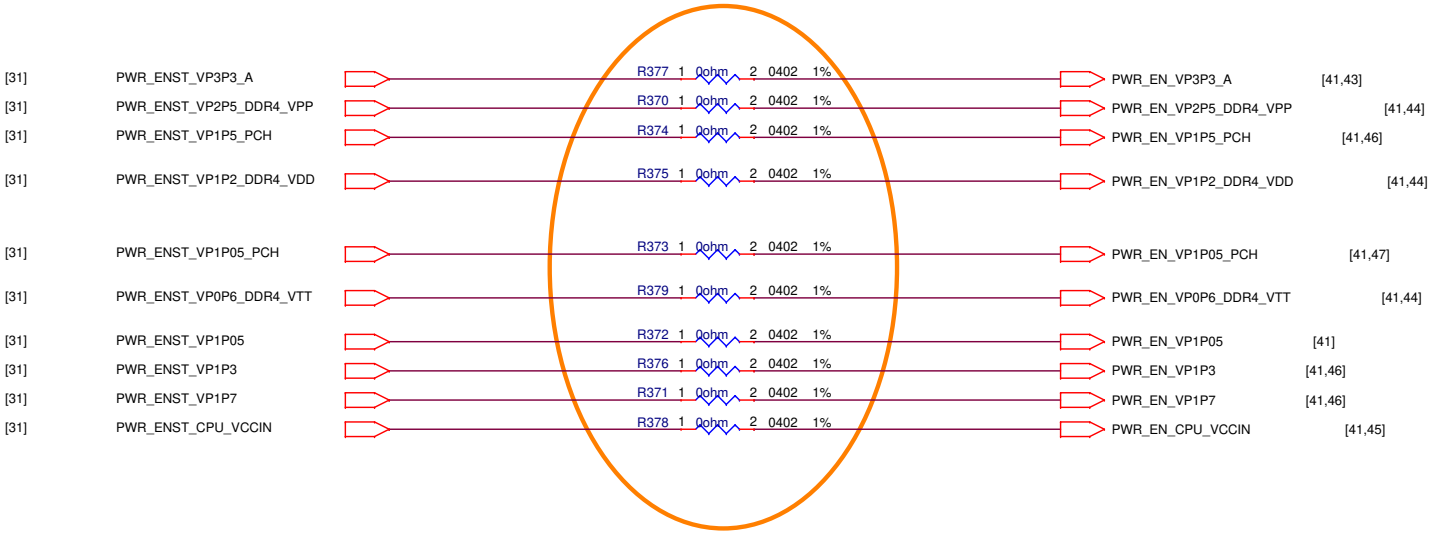

U31B
EPM1270F256I5N
VP3P3
VP2P5
VCCINT_CPLD
R364 1 0ohm 2 0402 1%
R365 1 0ohm 2 0402 1%
BOM = NI
[30] CMOS_CLR
[32] BUILD_ID0
[32] BUILD_ID1
[32] HW_REV_ID0
[32] HW_REV_ID1
R366 4.7Kohm 1% 0402
R367 4.7Kohm 1% 0402
R368 4.7Kohm 1% 0402
R369 1Kohm 1% 0402
J8
HS1105H-RN
SMT TYPE
JTAG_TCK
JTAG_TDO
JTAG_TMS
JTAG_TDI
[12,31,36]
R476 4.7Kohm 0402 1%
R477 0ohm 0402 1%
BOM = NI
CPU_ID
CPU_ID (CPU card identification)
0: Legacy BW-DE CPU board
1: New White Box BW-DE CPU board
Build ID [1:0] = 01
00 : 1
01 : 2
10 : 3
11 : 4
Hardware Revision [1:0]= 10
00: Proto
01: Alpha
10: Beta
11: PVT
SKU ID[3:0] = 0000
0000 : CSGR BW-DE CPU board
0001 : Reserved
0010 : Reserved
:
1111 : Reserved
[13] CPLD_RTCRST_L
R423 R424 R425 R426 2 4.7Kohm 0402 1% BOM = NI
R427 R428 R429 R430 2 NC_4.7Kohm 1% BOM = NI
R431 R432 R433 R434 R435 R436 R474 R475
[32] SKU_ID0
[32] SKU_ID1
[32] SKU_ID2
[32] SKU_ID3
U34_MR_R_L
[34]
<Core Design>
UfiSpace Co., Ltd.
Title
32. CPLD (2/4)
Document Number:
95.2801T00
PCB P/N:
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For compliance suggestion



5/10 Add 0 ohm resistors for power debug



<Core Design>

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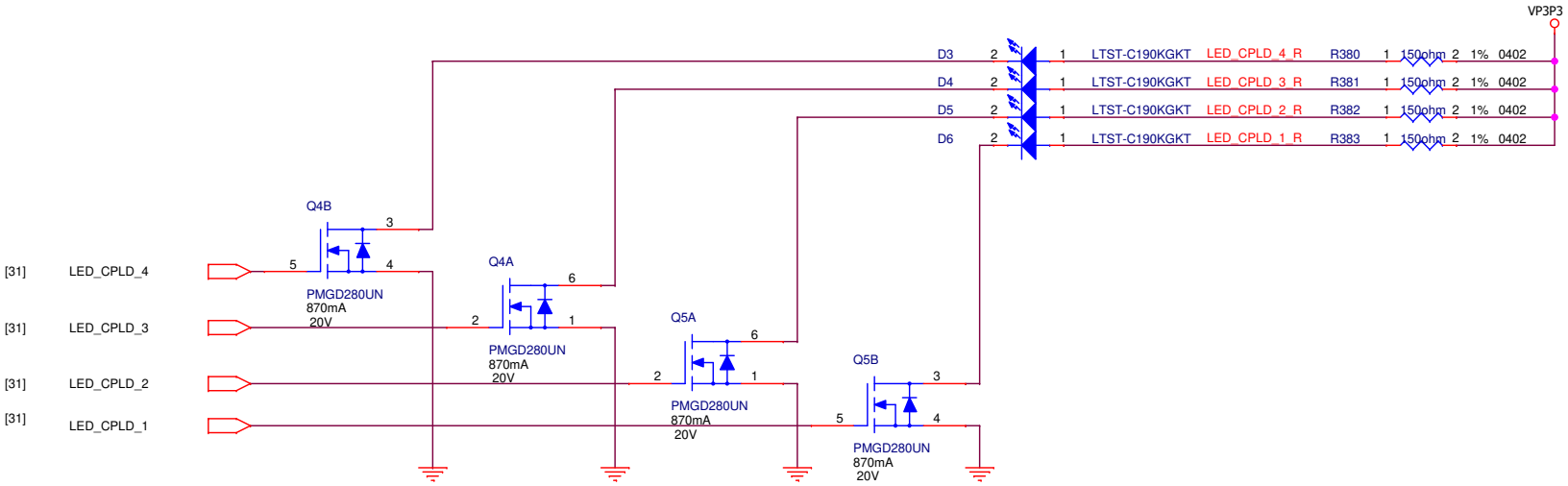
Title: 33. CPLD (3/4)

Document Number: 95.2801T00

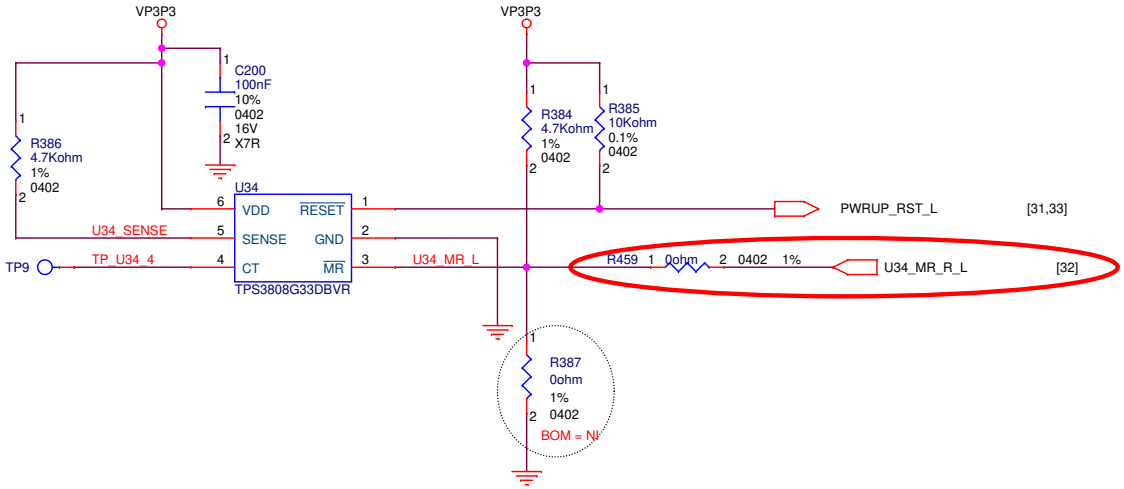
PCB P/N:

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Rev



CPLD RESET IC

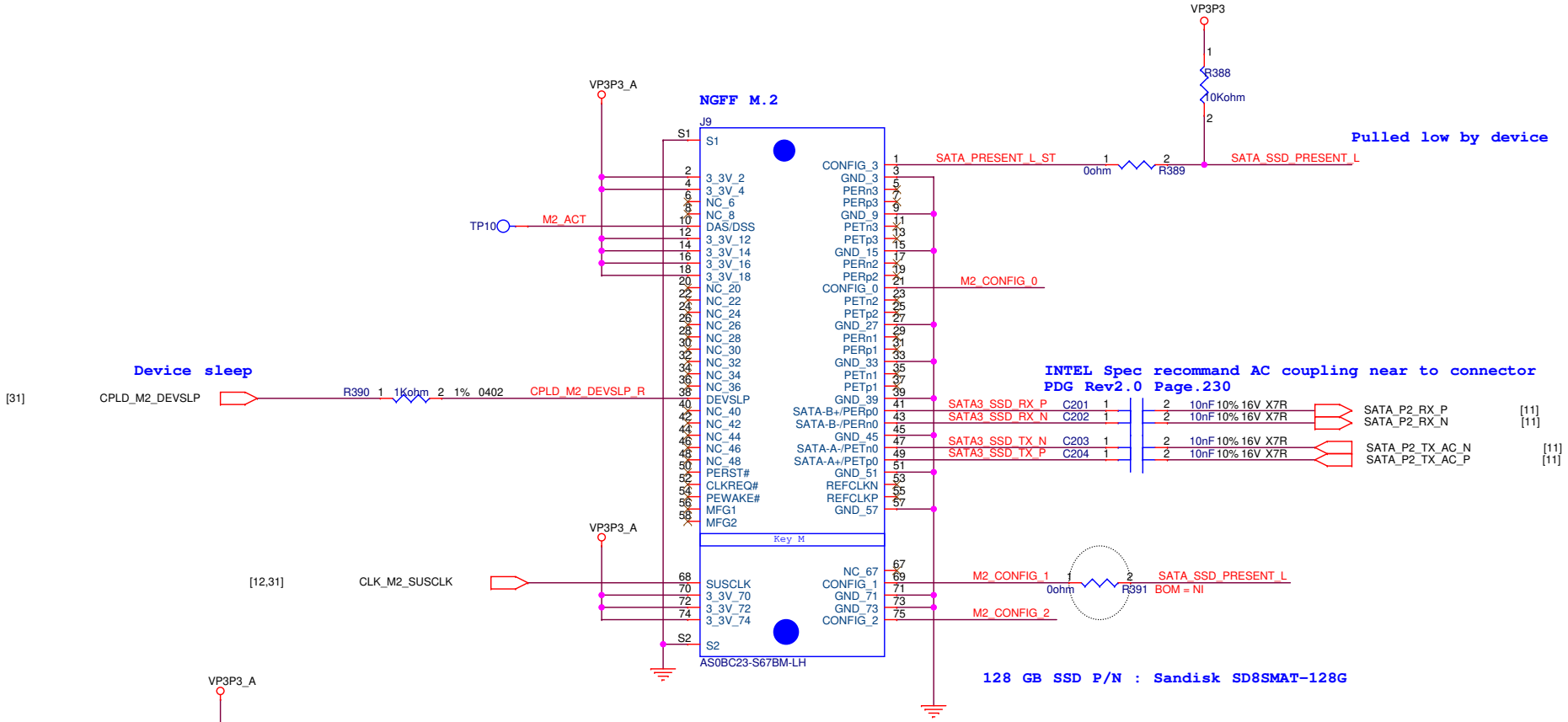


<Core Design>

UfiSpace Co., Ltd.

Title: 34. CPLD (4/4)

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<Core Design>

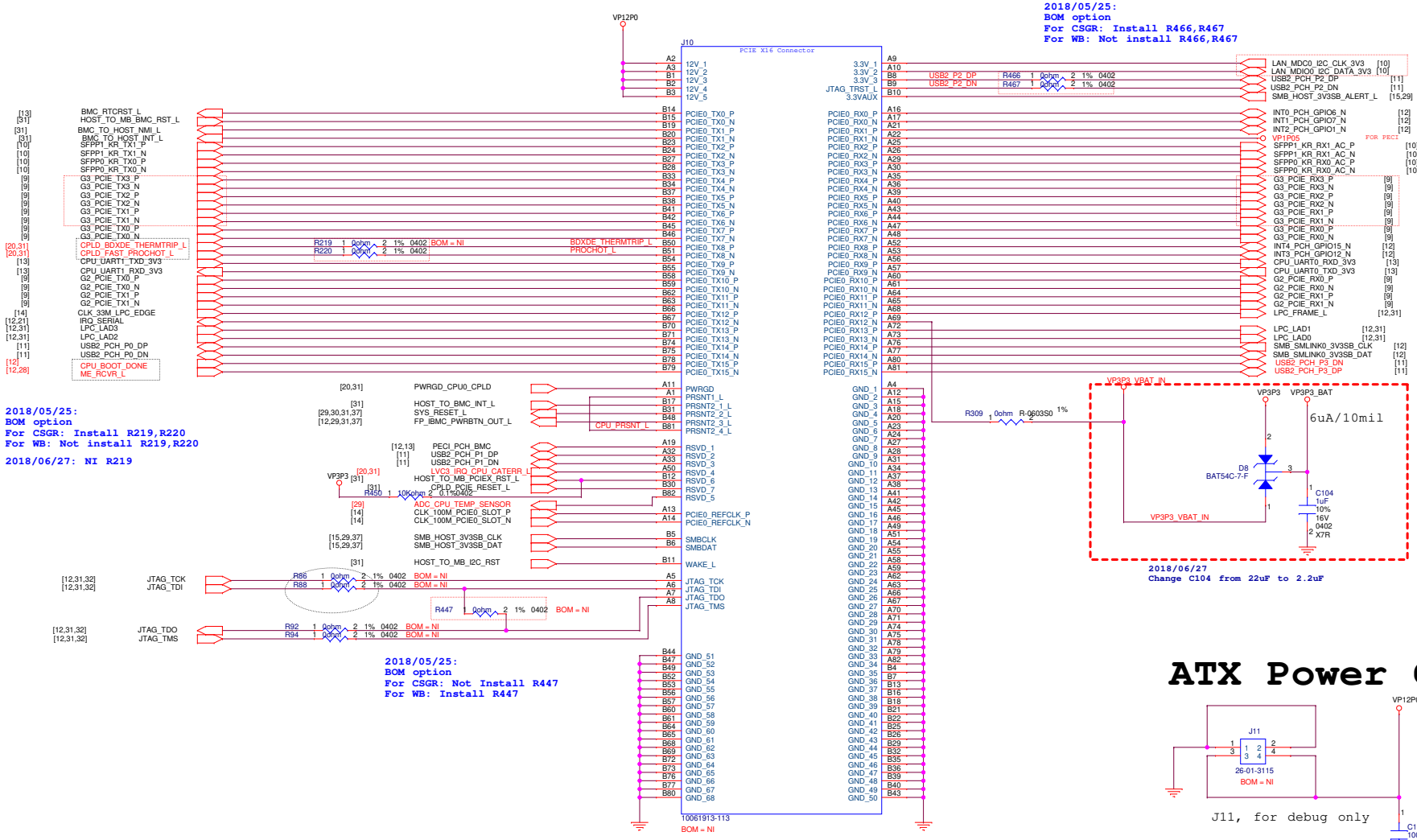
UfiSpace Co., Ltd.

Title

35. M.2 CONN

Document PCB P/N:	Number: 95.2801T00	Sheet 35 of 48	Rev

Gold Finger Connector



For PCIE and SGMII
CPU(TX)--->Finger(TX)--->Connector(TX)--->MAC(RX)
CPU(RX)<---Finger(RX)<---Connector(RX)<---MAC(TX)

ATX Power Connector

J11, for debug only

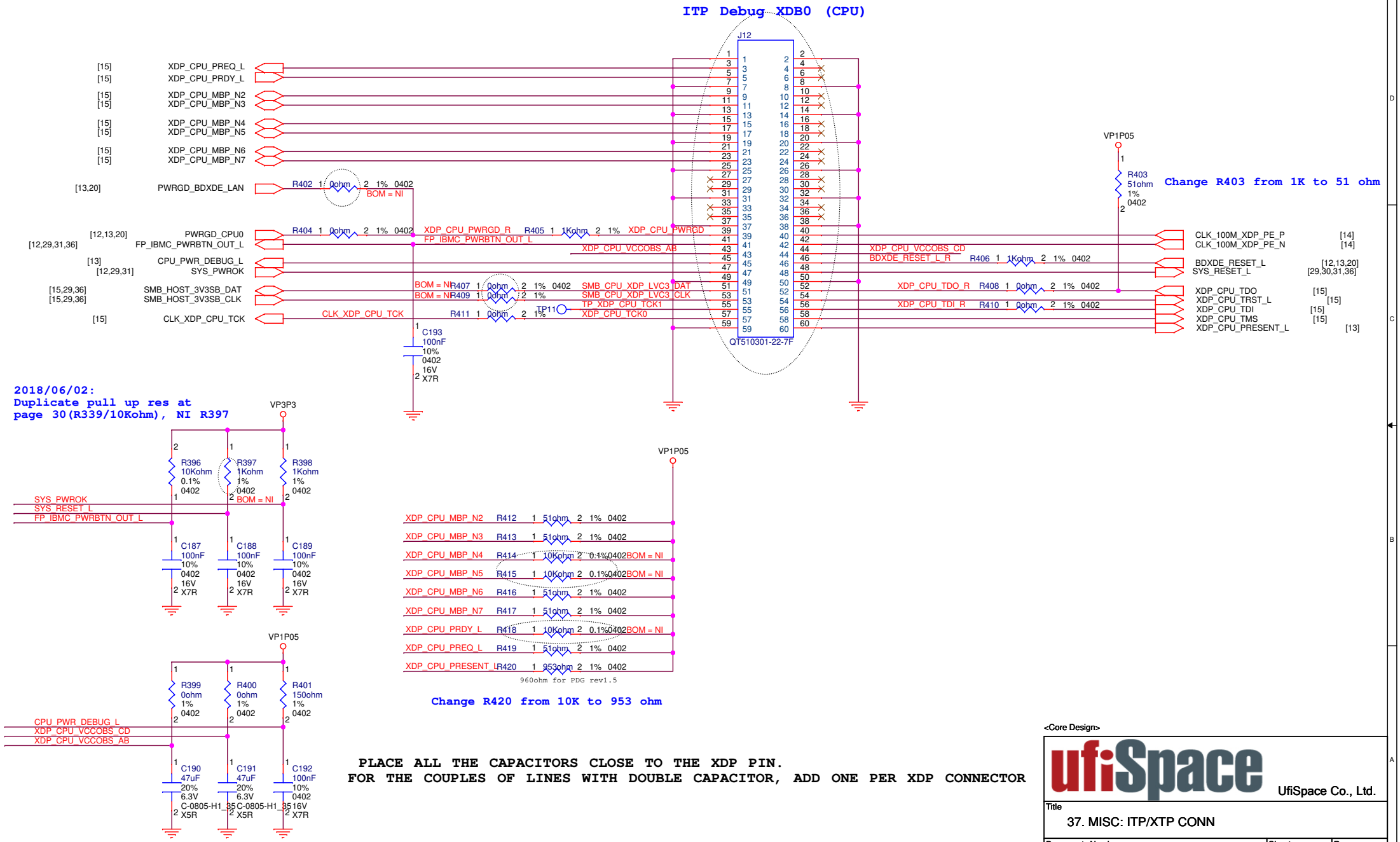
[CAD]: 20mil

<Core Design>
UfiSpace Co., Ltd.

Title: 36. GOLD FINGER CONN

Document Number:	Sheet	Rev
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ITP Debug XDB0 (CPU)



2018/06/02:
Duplicate pull up res at page 30(R339/10Kohm), NI R397

Change R420 from 10K to 953 ohm

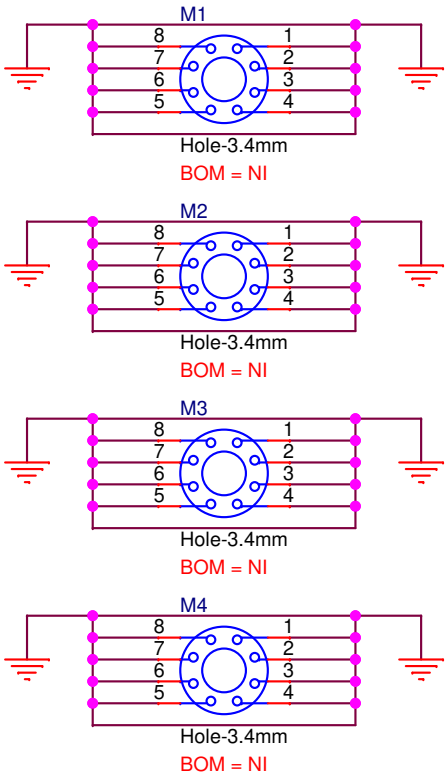
PLACE ALL THE CAPACITORS CLOSE TO THE XDP PIN.
FOR THE COUPLES OF LINES WITH DOUBLE CAPACITOR, ADD ONE PER XDP CONNECTOR

<Core Design>

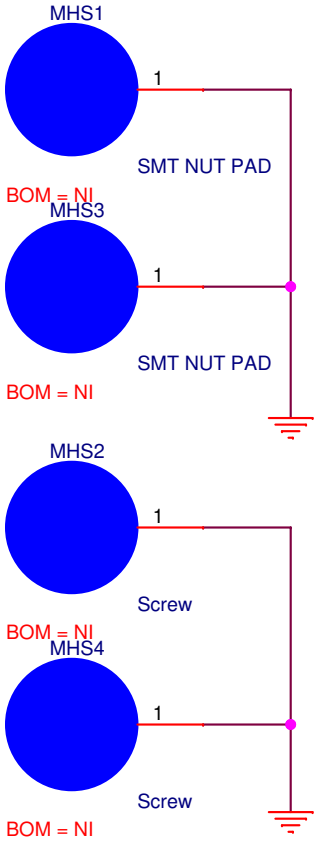
UfiSpace Co., Ltd.

Title: 37. MISC: ITP/XTP CONN

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SMT NUT for Heatsink Assembled



BOM ONLY PARTS

P/N: 503.00860.005 LABEL BLANK	P/N: 400.00727.015 HEAT SINK CPU
P/N: 309.00149.015 PCB	P/N: JSCPUBP7045-B BRACKET CPU
P/N: JSDHM24-A28M41 SSD 128GB	P/N: 401.00024.005 SCREW M2.5 4mm
P/N: JSM4DS-8GMSQW0 SODIMM 8GB	P/N: 484.00238.005 SPONGE EVA 62*9*6mm
P/N: JSM4DS-8GMSQW0 SODIMM 8GB	P/N: JS1345 AMI BIOS LABEL

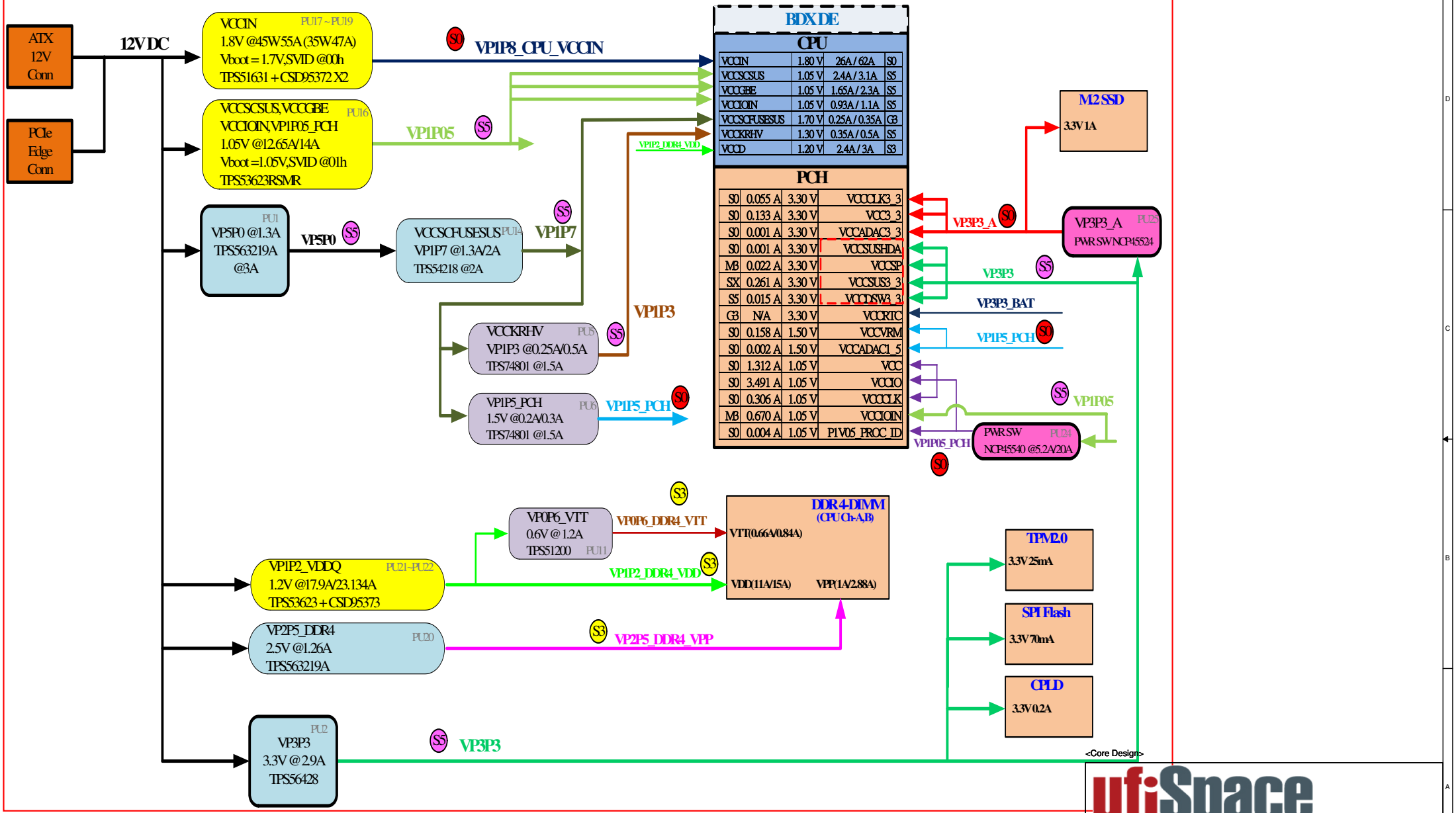
<Core Design>

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Title

38. MISCELLANEOUS

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Title: 39. POWER MAP

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INDEX	FUNCTION	MAX AMPS	LABEL	BASED ON	PAGE	INPUT
1	CPU_VCCIN_1.8V	55	VP1P8_CPU_VCCIN	TPS51631ARSMR	45	VP12P0
2	CPU_1.05V	14	VP1P05	TPS53623RSMR	47	VP12P0
3	CPU_1.7V	2	VP1P7	TPS54218RTER	46	VP5P0
4	CPU_1.3V	1.5	VP1P3	TPS74801DRCR	46	VP1P7
5	CPU_PCH_1.05V	14	VP1P05_PCH	NCP45540IMNTWG-H	47	VP1P05
6	CPU_PCH_1.5V	1.5	VP1P5_PCH	TPS74801DRCR	46	VP1P7
7	DDR4_1.2V	23	VP1P2_DDR4_VDD	TPS53623RSMR	44	VP12P0
8	DDR4_0.6V	1.2	VP0P6_DDR4_VTT	TPS51200DRCT	44	VP1P2_DDR4_VDD
9	DDR4_2.5V	1.26	VP2P5_DDR4_VPP	TPS563219A	44	VP12P0
10	5.0V STBY	1.3	VP5P0	TPS563219A	42	VP12P0
11	3.3V STBY	3	VP3P3	TPS56428DDAR	43	VP12P0
12	3.3V	3	VP3P3A	NCP45524IMNTWG-H	43	VP3P3

<Core Design>

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Title: 40. POWER TABLE

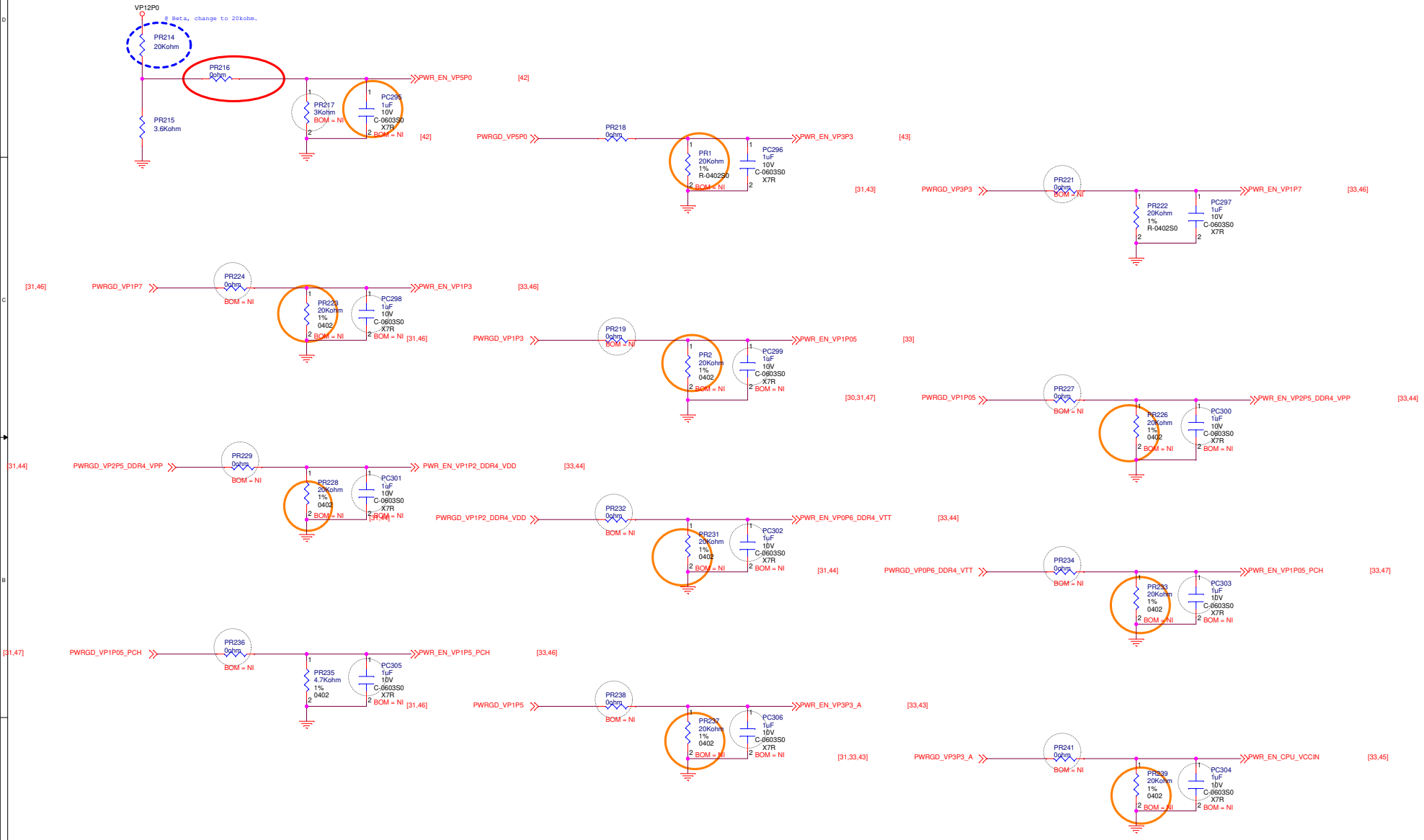
Document Number: 95.2801T00

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Power up Sequence



<Core Design>

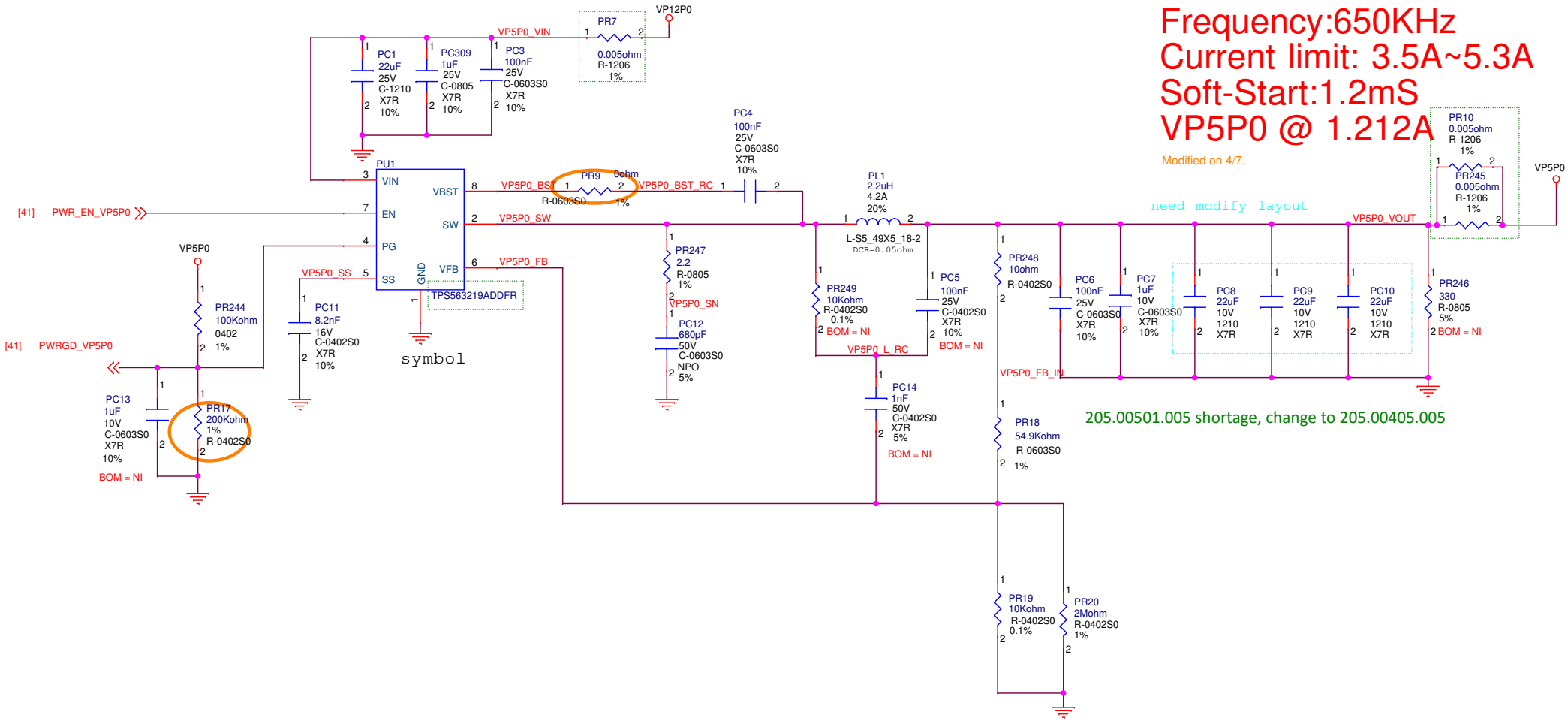
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Title: 41.POWER SEQUENCE

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Rev



<Core Design>

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Title

42. 5V

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PCB P/N:

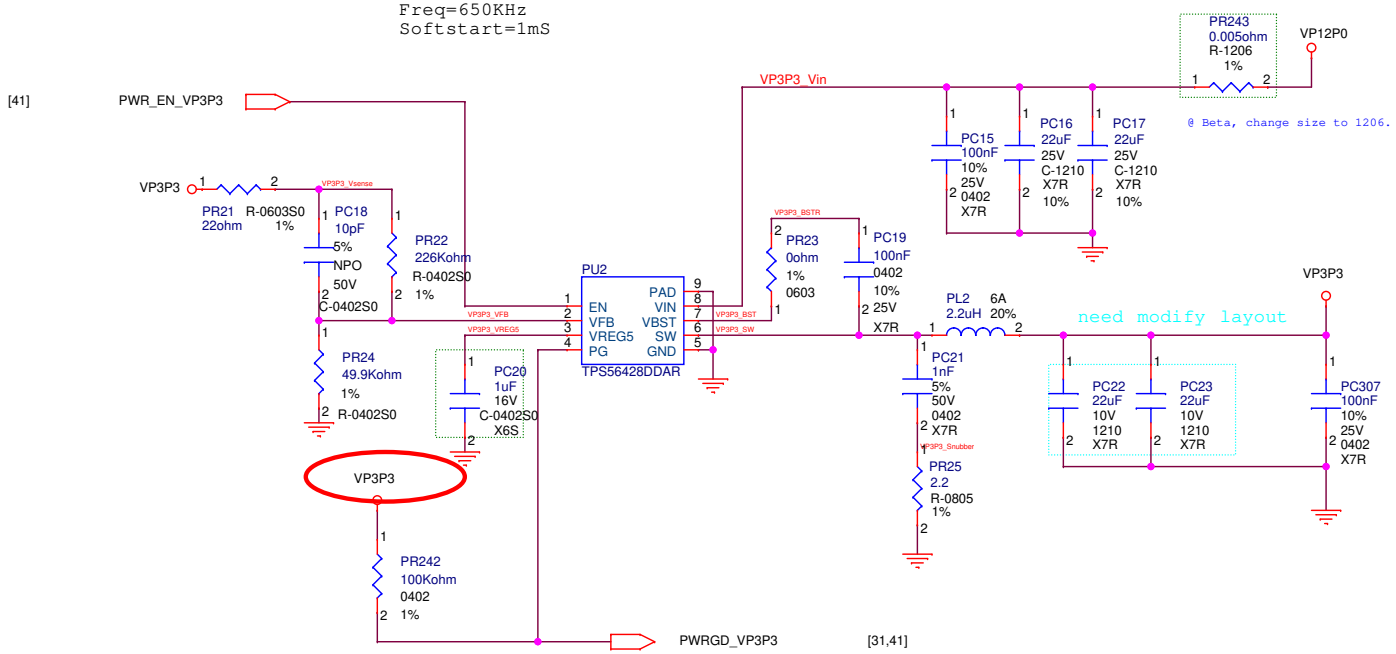
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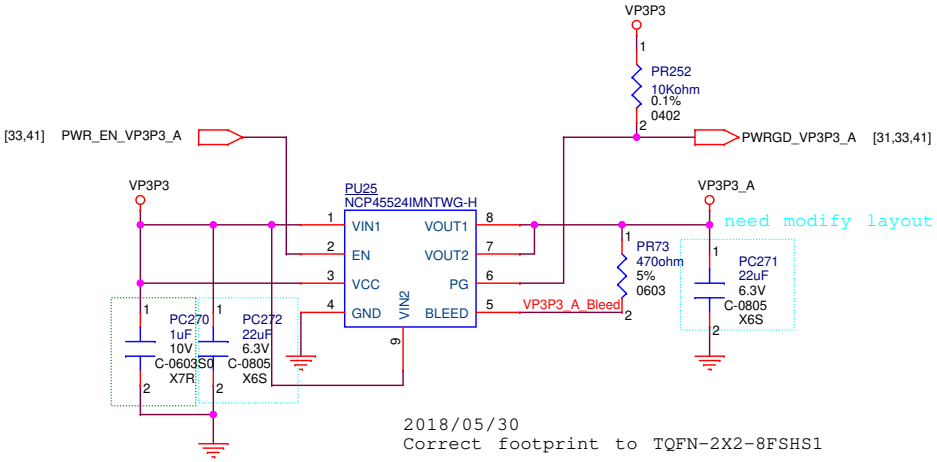
VP3V3 TPS56428 @ 2.886A

Modified on 4/7.

Vo=0.6V*(1+PR22/PR24)=3.317V
OCP=5.6A
Freq=650KHz
Softstart=1mS



VP3P3_A NCP45524



CAD NOTE:
Add divider circuit can make Enable pin not floating, and to avoid turn on /turn off error action.

<Core Design>

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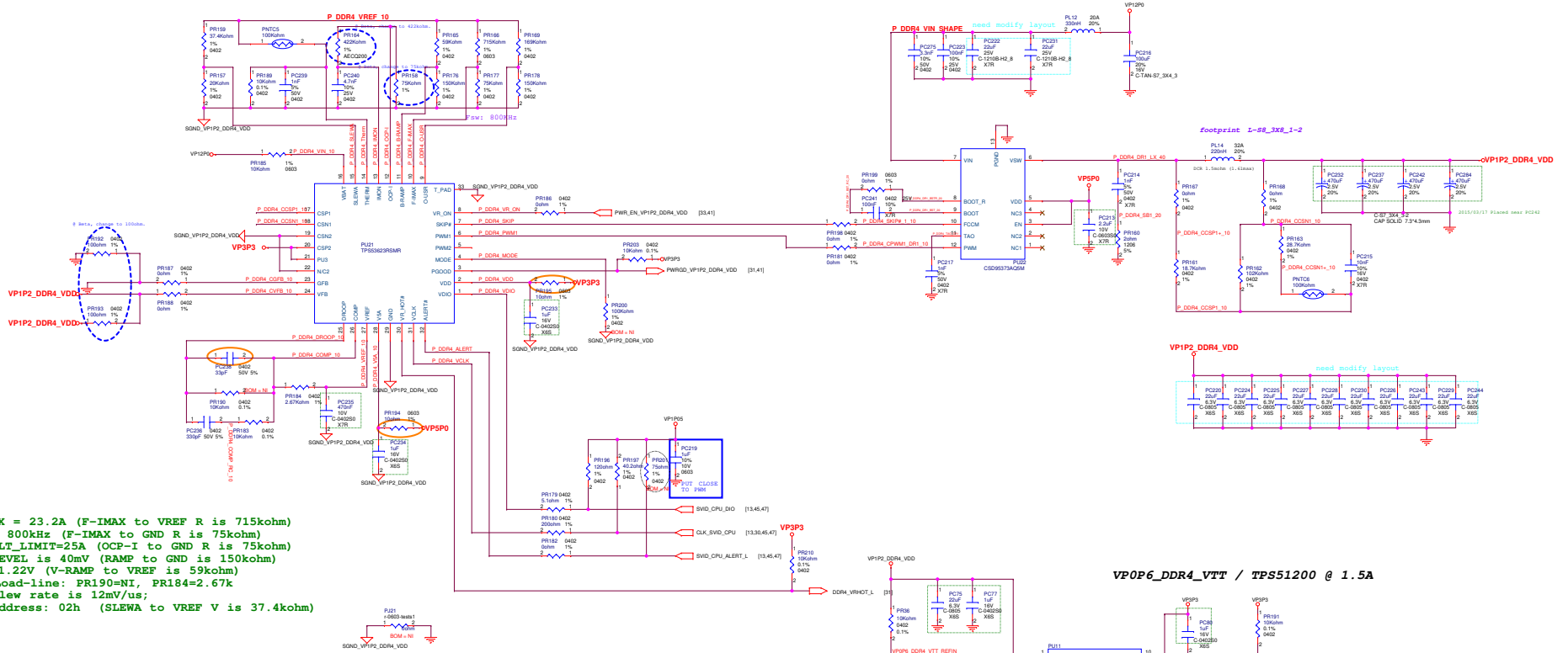
Title: 43. 3.3V

Document Number: 95.2801T00
PCB P/N:

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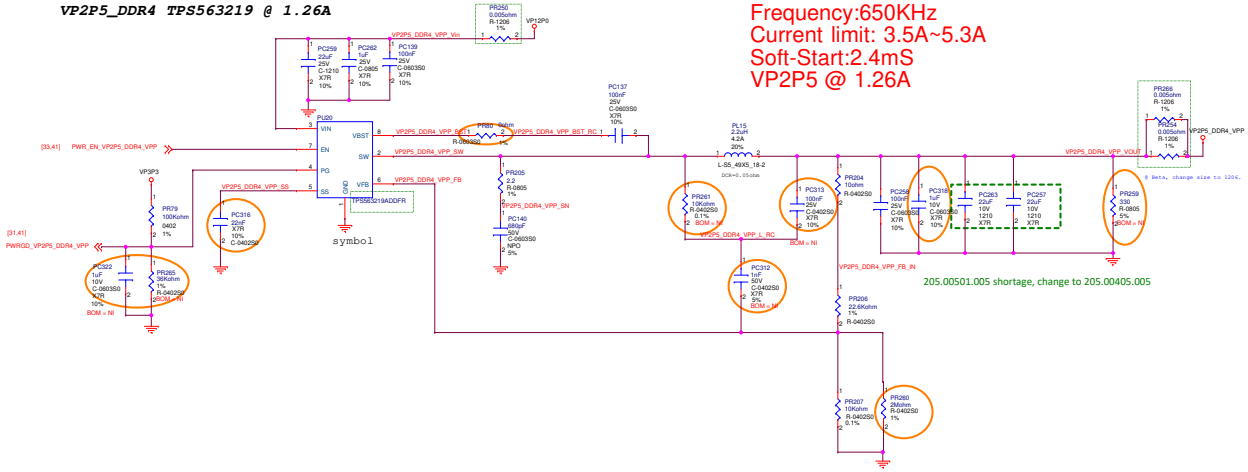
Rev

VP1P2_DDR4_VDD TPS53623 @ 22.934Amax (17.9A TDC)



1. ICC_MAX = 23.2A (F-IMAX to VREF R is 715kohm)
2. Freq = 800kHz (F-IMAX to GND R is 75kohm)
3. OC_FAULT_LIMIT=25A (OCP-I to GND R is 75kohm)
4. RAMP LEVEL is 40mV (RAMP to GND is 150kohm)
5. VBOOT=1.22V (V-RAMP to VREF is 59kohm)
6. Zero Load-line: PR190=NI, PR184=2.67k
7. Vout slew rate is 12mV/us;
8. SVID Address: 02h (SLEWA to VREF V is 37.4kohm)

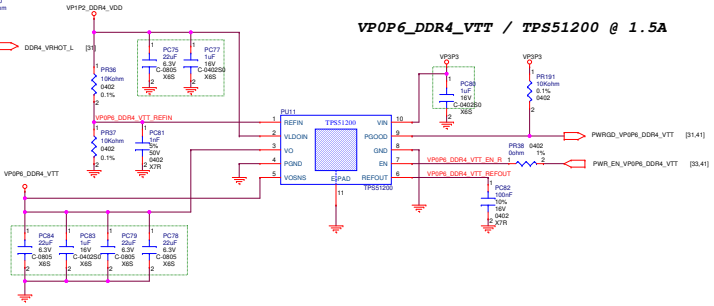
VP2P5_DDR4 TPS563219 @ 1.26A



Frequency:650KHz
Current limit: 3.5A~5.3A
Soft-Start:2.4mS
VP2P5 @ 1.26A

205.00501.005 shortage, change to 205.00405.005

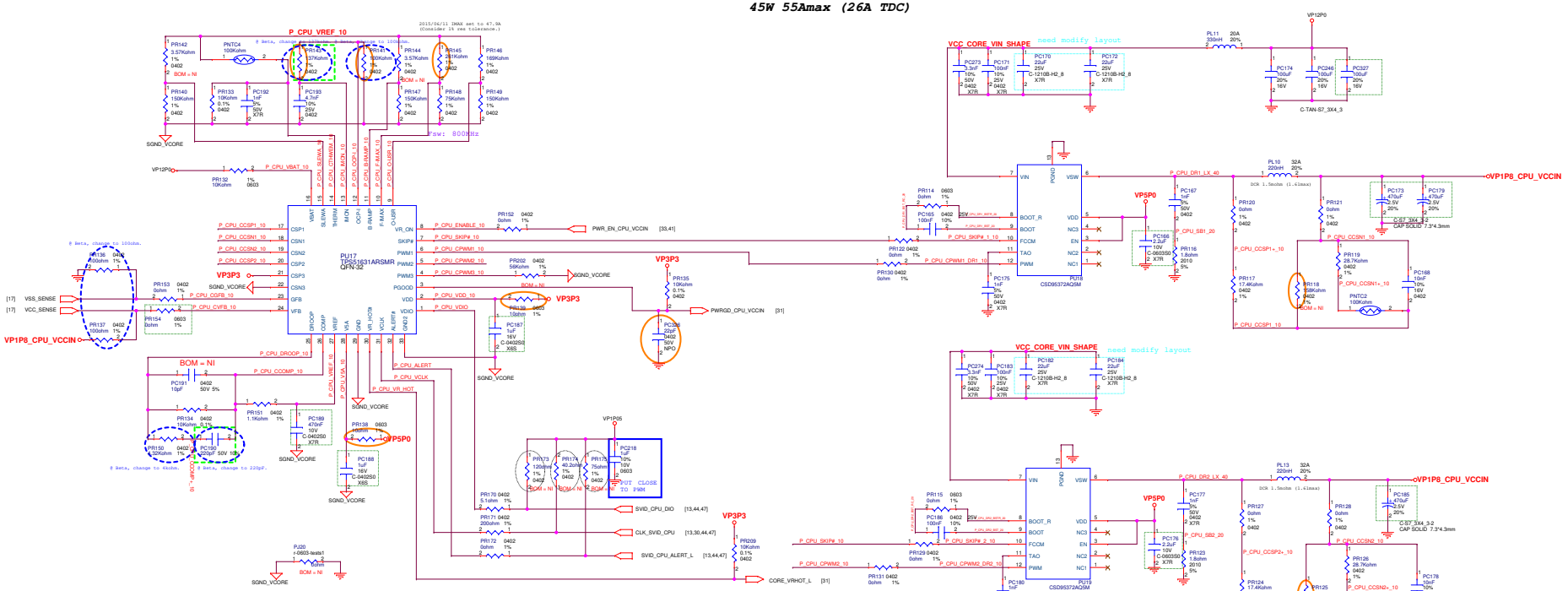
VP0P6_DDR4_VTT / TPS51200 @ 1.5A



<Core Design>
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UfiSpace Co., Ltd.

Title	44. 2.5V / 1.2V / 0.6V		
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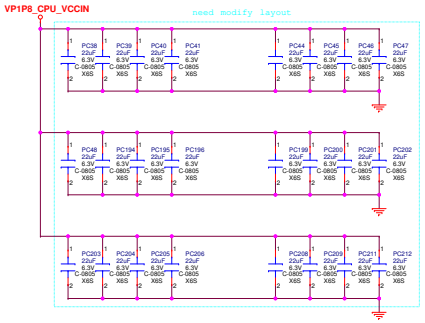
VCC_Core TPS51631A @ 25W 34Amax (15A TDC)
35W 47Amax (21A TDC, OCP set to 65A)
45W 55Amax (26A TDC)



1. ICC_MAX = 57A (F-IMAX to VREF R is 261k)
2. Freq = 800kHz (F-IMAX to GND R is 75kohm)
3. OC_FAULT_LIMIT=70A (OCP-I to GND R is 100kohm)
4. RAMP LEVEL is 40mV (RAMP to GND R is 150kohm)
5. VBOOT= 1.7V (RAMP to VREF R is OPEN)
6. Load-line: 1.5mV/A (PR151 is 1.1kohm)
7. Vout slew rate is 20mV/us (SLEWA to GND R is 150kohm)
8. SVID Address: 00h (SLEWA to VREF R is OPEN)
9. OSR disable (PWM3 to GND R is OPEN)

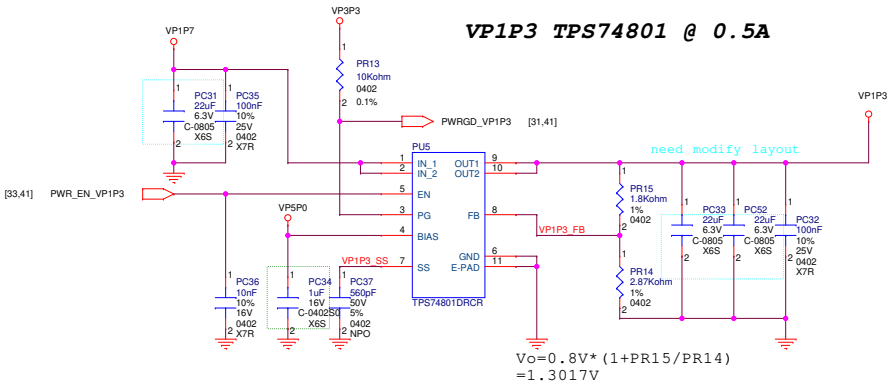
NI these two resistors to enable PWM2





<Core Design>
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UfiSpace Co., Ltd.
Title
45. 1.8V
Document Number: 95.2801T00
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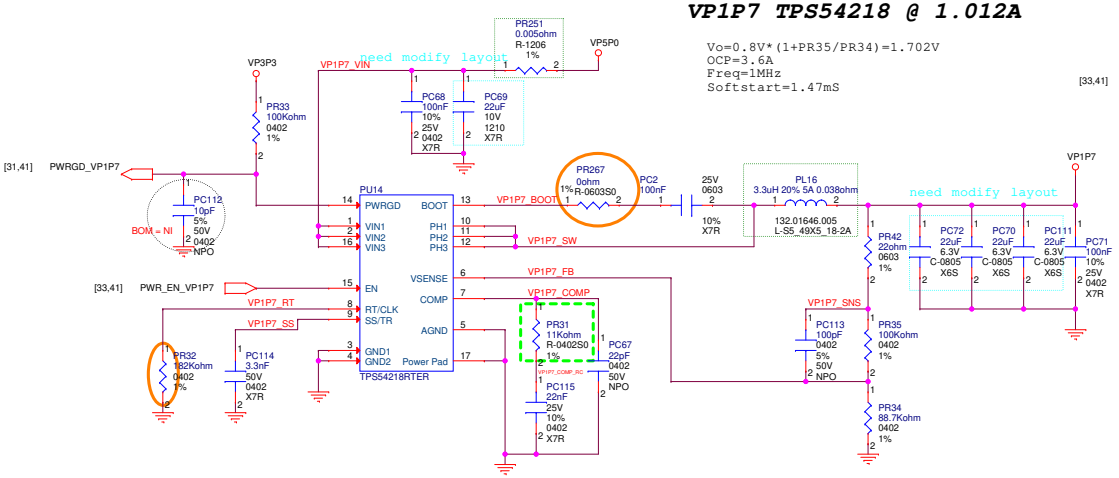
VP1P3 TPS74801 @ 0.5A



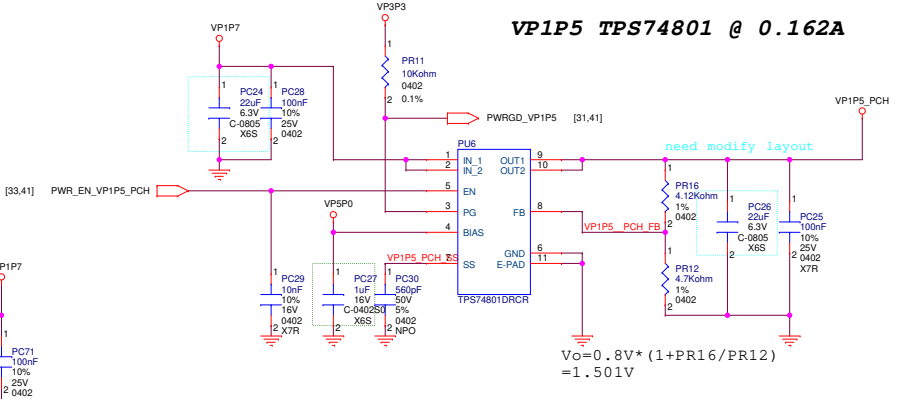
Vo=0.8V*(1+PR15/PR14)
=1.3017V

VP1P7 TPS54218 @ 1.012A

Vo=0.8V*(1+PR35/PR34)=1.702V
OCP=3.6A
Freq=1MHz
Softstart=1.47mS



VP1P5 TPS74801 @ 0.162A



Vo=0.8V*(1+PR16/PR12)
=1.501V

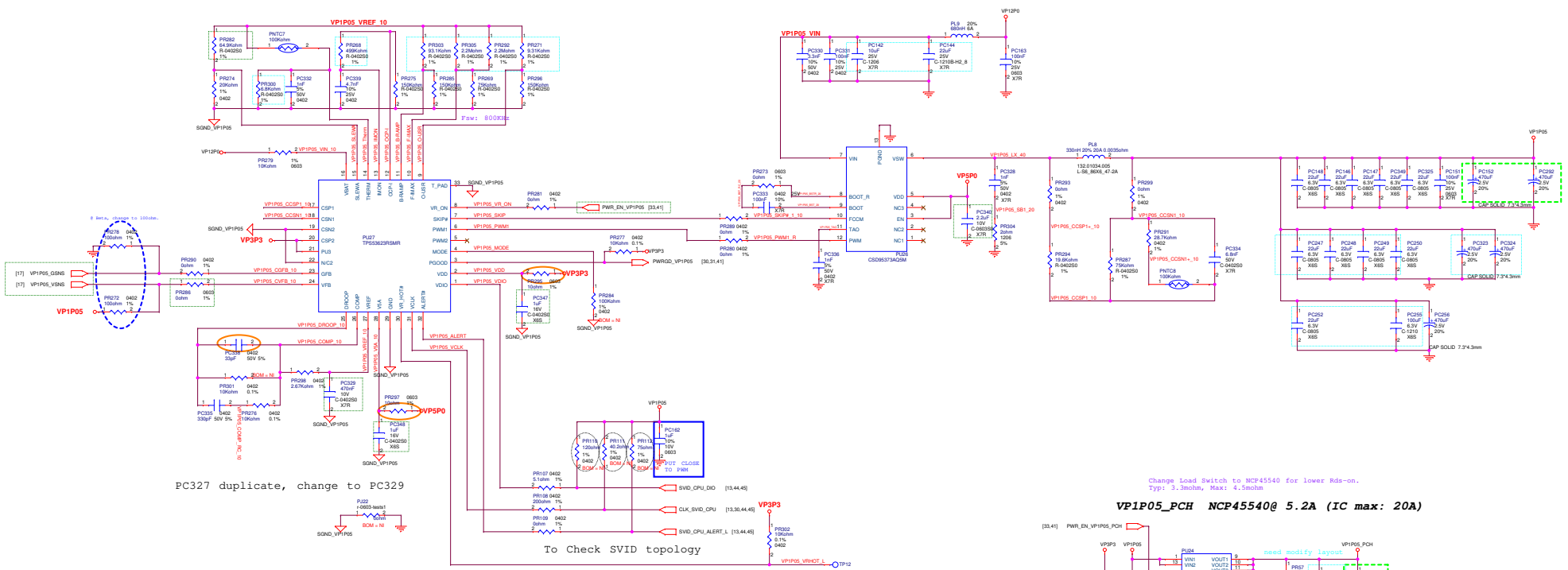
<Core Design>

UfiSpace Co., Ltd.

Title
46.1.7V / 1.5V / 1.3V

Document Number: PCB P/N: 95.2801T00	Sheet 46 of 48	Rev

VP1P05_Combined @ 14Amax (12.65A TDC)



1. ICC_MAX = 15.2A (F-IMAX to VREF R is 1100k)
2. Freq = 800kHz (F-IMAX to GND R is 75kohm)
3. OC_FAULT_LIMIT=20A (OCP-I to GND R is 150kohm)
4. RAMP LEVEL is 40mV (RAMP to GND is 150kohm)
5. VBOOT=1.049V (V-RAMP to VREF is 93.1kohm)
6. Zero Load-line: PR301=NI, PR298=2.67k
7. Vout slew rate is 12mV/us;
8. SVID Address: 01h (SLEWA to VREF V is 64.9kohm)

<Core Design>
ufiSpace
UfiSpace Co., Ltd.

Title: 47. 1.05V			
Document Number: PCB P/N: 95.2801T00		Sheet 47 of 48	Rev

REVISION HISTORY:

<Core Design>

UfiSpace Co., Ltd.

Title

48. HISTORY

Document Number: / PCB P/N:	Sheet	Rev
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